Microelectronics Journal 46 (2015) 415–421

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# A 5-GHz LC VCO with digital AAC and AFBS for 2.4 GHz ZigBee transceiver applications

Di Li*, Yin-Tang Yang, Zhang-Ming Zhu, Zuo-Chen Shi

*School of Microelectronics, Xidian University, No.2 South Taibai Road, Mailbox 373, Xi'an, Shaanxi 710071, China*

ARTICLE INFO

*Article history:*
Received 1 December 2014
Received in revised form
14 March 2015
Accepted 24 March 2015
Available online 9 April 2015

*Keywords:*
Voltage-controlled oscillator
Automatic amplitude control
Frequency-band
Selection
ZigBee
IEEE802.15.4

ABSTRACT

A 5 GHz LC VCO (voltage-controlled oscillator) with automatic amplitude control (AAC) and automatic frequency-band selection (AFBS) for 2.4 GHz ZigBee transceivers is presented. Instead of continuous feedback loop, an alternative amplitude calibration scheme is proposed in this paper to alleviate the deficiencies inherent in the conventional approach. It helps to keep the VCO at optimum amplitude to avoid saturation of the cross-coupled transistors and therefore stabilizes the phase noise performance over process, voltage and temperature variations. For the ZigBee application with 16 frequency channels, a coarse tuning loop is added in this work to implement the frequency-band selection using the AFBS mechanism. The VCO core and the digital AAC, AFBS modules have been fully integrated in a 2.4 GHz ZigBee transceiver which was fabricated in a 0.18 μm RF-CMOS technology. The current consumption is 4.7 mA at 4.85 GHz with 1.8 V power supply and a chip area of about 0.285 $mm^2$ is occupied. The VCO is capable of operating from 4.67 GHz to 5.18 GHz and the measured phase-noise level is −120 dBc/Hz at 1 MHz offset from a 4.85 GHz carrier. The tuning sensitivity $K_{VCO}$ of the VCO is about 78 MHz/V with 0.9 V control voltage.



## 1. Introduction

The ZigBee/IEEE802.15.4 which is an industry standard for low-cost, low-power and low-rate wireless applications has been studied widely and deeply for several years. It assigns three unlicensed industrial, scientific and medical (ISM) operation frequency bands: 815 MHz, 915 MHz and 2.4 GHz respectively [1–4]. Especially, 2.4 GHz is the most attractive band since it is available throughout the world. The transceiver for 2.4 GHz ZigBee generally adopts Low-IF receiver scheme to avoid sensitivity reduction due to flicker noise and direct-conversion scheme for transmitter to save chip area and power consumption. As an indispensable and key building block, the frequency synthesizer provides local oscillator (LO) signals to both the receiver and transmitter paths for mixing with the carrier. The VCO (Voltage-controlled oscillator) is the most critical block in the synthesizer and operates at the highest frequency which is about twice of the channel frequency in the transceiver. In terms of phase noise and tuning range, the VCO performance determines basic performance characteristics of a transceiver [5–7].

For the popular current-biased LC-VCO, the oscillation amplitude varies over its tuning range and cause detrimental variations in the phase noise performance over frequency. Meanwhile, steady-state oscillation amplitude set the amplitude to a predefined level so the operation of the frequency dividers in the PLL (Phase-Locked Loop) is not compromised. The amplitude variation also has a significant impact on neighboring system blocks, such as a mixer where the conversion gain would vary if the VCO amplitude changes widely, or a prescaler that interfaces to the VCO [5,8–10]. It can be concluded that providing a way to control the oscillation amplitude is highly desirable. Conventional methods for controlling the amplitude of the VCO output are generally employing an analog AAC scheme where oscillation amplitude is controlled by a continuous-time feedback loop and have been successfully demonstrated in references [11–13]. However, the crucial and effective role in sustaining the oscillation amplitude comes at the cost of added complexity and a noise penalty due to the presence of additional noise contributors that feed back to the oscillator. This work proposes an alternative digital AAC scheme to adjust the oscillation amplitude of the VCO.

The PHY of the unlicensed 2.4 GHz band defines sixteen frequency channels ranging from 2.4 GHz to 2.4835 GHz with channel spacing 5 MHz [14–15]. The RF (Radio Frequency) of channel $k$ is given by:

$$F_{channel,k} = [2405 + 5(k-11)]MHz \tag{1}$$

where $k=11,12,\ldots,26$. The base-band frequency of the ZigBee receiver is chosen as 2 MHz in this design, and therefore, the LO

* Corresponding author. Tel.: +86 13709250163; fax: +86 2988202562.
*E-mail address:* lidi2004@126.com (D. Li).

http://dx.doi.org/10.1016/j.mejo.2015.03.017
0026-2692/

(local oscillator) frequency provided for the receiver should be 2 MHz lower than the channel center frequency for a low-IF scheme. E.g. if the channel number is 11, the channel center frequency $F_{channel,k}$ is 2.405 GHz, and then, a 2.403 GHz LO is required to realize the 2 MHz intermediate frequency(IF). Since the VCO operates at twice the carrier frequency to avoid the leakage of the oscillator, 4.806 GHz should be generated by the VCO. The LO of channel $k$ can be given by:

$$F_{LO,k} = [4806 + 10(k-11)]\,\text{MHz} \quad (2)$$

For the sixteen oscillation frequencies ranging from 4.806 GHz to 4.956 GHz, it is wisdom and necessary to provide an automatic frequency band selection (AFBS) scheme to the multi-bands VCO targeting for the ZigBee applications.

## 2. VCO with digital AAC

Although ring- or relaxation-type oscillators can be found in some applications, their poor phase noise performance, larger power consumption and chip area compared to the differential LC (Inductor and Capacitor) VCOs disqualify them in most RF applications. In the topologies of LC-VCOs, the complementary cross-coupled VCO has better noise performance than NMOS-only cross-coupled VCO [5,8]. Conventional analog AAC in LC-VCOs adopts an analog negative feedback loop to tune the tail current of the LC VCO as shown in Fig. 1. For a LC-VCO with parallel tank resistance of $R_{tank}$, the peak voltage developed across the LC tank differentially can be given by:

$$V_p = \frac{1}{T}\int_0^T I_P\ \sin(wT)R_{\tan\ k}dt = \frac{1}{2\pi}\int_0^{2\pi} I_P\ \sin(wT)R_{\tan\ k}dt = \frac{2I_pR_{\tan\ k}}{\pi} \quad (3)$$

where $I_p$ is the peak value of the current flowing across the tank.

It is obvious that, the current and therefore the amplitude in the VCO are set by the current source. The AAC module contains a current mirror to produce the tank current which is taken by the VCO core and produce an output voltage proportional to the input tank current [16]. With the AAC loop, if the amplitude is increased for example, the tail current $I_{bias}$ would be decreased, which leads to a decrease in the oscillation amplitude. However, the tail current source implemented by transistors increases the supply voltage budget and injects the AAC circuit noise into the VCO. The injected AAC noise is up converted at the VCO output and leads to higher VCO phase noise.

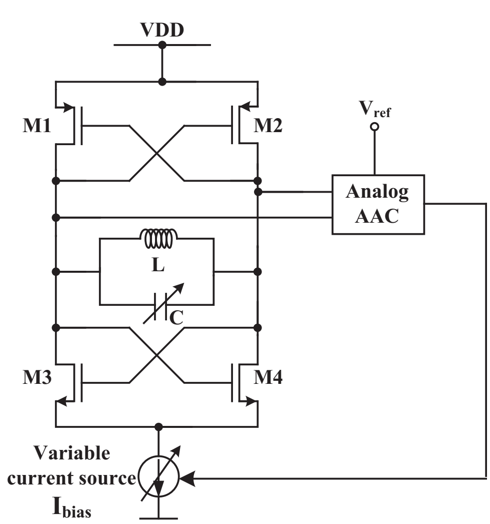


**Fig. 1.** Conventional complementary VCO with analog AAC feedback loop.

In this work, an alternative amplitude control scheme is proposed to alleviate the deficiencies inherent in the conventional approach. Instead of continuous feedback loop and current source scheme, a calibration approach and switched-resisters arrays are used as shown in Fig. 2. The VCO core consists of two switched-resistors arrays ($B_R$ and $B_T$), LC tank, varactors array and cross-coupled transistors. The $B_R$ in the VCO core is in fact a replica of the one in the bias and meanwhile, they are controlled by the same digital bits $d$[5:0]. The current of the bias $I_{ref}$ is controlled by a 3-bit control word from the registers which provides a 6-bit control word to the switched resistors array $B_R$ by a control bits generator. Then, the output from the VCO core is low-pass filtered and compared with the reference voltage $V_{bias}$ With the comparison result, the digital AAC, which is in fact a simple digital state machine, generates a 6-bit control word to the switched-resistors array $B_T$ to tune the voltage $V_t$. With the use of this feedback loop, the two dc voltages $V_t$ and $V_{bias}$ track very well over process and temperature. Since the $B_R$s in the VCO core and bias have the same resistance with same control bits, current of the VCO core $I_{vco}$ equal to the current of the bias $I_{ref}$. This method has the advantage of being active only during calibration and therefore, the steady-state phase noise performance of the VCO is not affected. Furthermore, the power consumed by calibration circuits is negligible since they are powered off as soon as calibration ends.

Fig. 3 shows the schematic of the current tunable bias. The array $B_R$ is implemented by a set of six weighted resistors with transistor switches to make the resistance adjustable. Similarly, the current sources array is also implemented by a set of four weighted current sources to make the current adjustable. There is a negligible voltage drop across each of these switch transistors because they works in the deep triode region. The switches controlled by $d$[5:0] and $D$[2:0] provide respectively 64 and 8 possible settings for the values of the resistance and current. The control bit applied to switch transistor M10 which is

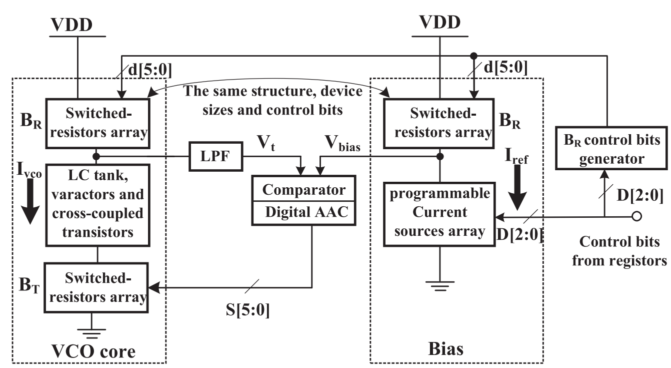


**Fig. 2.** Simplified structure of the LC VCO with digital AAC loop used in this design.

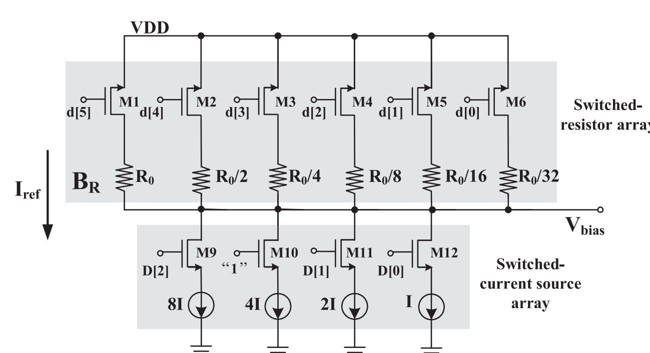


**Fig. 3.** Schematic of the current tunable bias.