Microelectronics Journal 46 (2015) 273–284

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

An all-digital semi-blind clock and data recovery system

Mina Abdallah *, Ahmed Eladawy *, Ahmed Mohieldin *

Electronics and Electrical Engineering Department, Cairo University, Giza 12613, Egypt

ARTICLE INFO

Article history:
Received 20 January 2014
Received in revised form
23 December 2014
Accepted 27 January 2015
Available online 18 February 2015

Keywords:
CDR
ADPLL
OC-192
Jitter

ABSTRACT

This paper presents a digitally intensive semi-blind clock and data recovery (SBCDR) system. The paper covers the theory, analysis, and system level simulation of this SBCDR. The proposed CDR is tailored to target the optical network standard OC-192. The SBCDR can provide the required jitter tolerance (JTo), and still provide enough jitter filtering to achieve the jitter transfer (JTr) requirements. Also, the recovered clock achieves a low jitter generation (JG) of 0.01 UI_{rms} and 0.0064 UI_{rms} for both the wide-band and high-band jitter filters defined by the standard. The proposed SBCDR provides two advantages over typical SBCDRs and PLL-based CRDs that target OC-192. First, the digitally intensive nature provides a scalable and process tolerant design. Second, the architecture provides a CDR that can pass all three jitter performance metrics, without the aid of an external clean-up phase locked loop (PLL) or a high performance clock multiplication unit (CMU) typically required by OC-192 transceivers. By utilizing a circular representation for the phase calculation in the over-sampling clock and data recovery (OSCDR), extensive pipe-lining in the implementation and higher data rate tolerance can be achieved. The simulation results of the proposed SBCRD agree closely with theoretical results.

1. Introduction

For a new CDR architecture, the implementation technology and the targeted standard have to be in mind. As CMOS device sizes scale down both requirements are getting more difficult. CMOS scaling enhances the performance of digital circuitry in terms of speed, area, and power consumption. On the other hand, analog circuitry suffers many impairments. Some of these impairments are less controllable technology variations, drop in transistor intrinsic gain, and increase of the added noise by the circuitry. There are two main architectural trends in circuits/systems designed to tackle these impairments. The first is to move as much as possible of the analog circuitry functionality to digital counterparts. The second is a design approach that supplements the analog circuitry with extra calibration, control, and aiding digital circuitry. Our proposed CDR system adopts these design trends up to the abstract architectural level.

The second architecture requirement is the target application. As digital circuitry advances, data demand increases dramatically and the data transfer rate also increases. This requires faster CDR and receiving circuitry. Also the standards governing this data transfer are getting more complex. A CDR performance is judged based on three jitter based metrics. Jitter tolerance (JTo) is always applicable for any CDR. The other two metrics, jitter transfer (JTr) and jitter generation (JG) LT are applicable when the recovered clock is re-used in transmitting data out. The target application OC-192 has a JTo mask with a highest corner frequency of 4 MHz, a JTr bandwidth of 120 kHz, and a JG of 0.03 and 0.01 UI_{PP} for two defined jitter integration filters [1–3]. The typical OC-192 utilizes a phase locked loop (PLL) CDR. A simplified block diagram of the PLL-CDR is shown in Fig. 1. The stand-alone CDR meeting JTo mask cannot achieve either the JTr or the JG. Additional high performance clock multiplication unit (CMU) is typically used as a supplement to the CDR to achieve all three jitter metrics. If the CMU cannot achieve the required jitter clean-up for the CDR and the required bandwidth control an extra clean up PLL is needed [4–6]. A simplified block diagram of the required timing macros for both cases is shown in Fig. 2.

2. Semi-blind CDR (SBCDR)

One of the intensively digital CDR architecture is the over-sampling CDR (OSCDR) [7]. It samples the received data at a rate higher than the data rate. A digital phase picking algorithm selects which sample is the optimum to be used as the received data. The OSCDR architectures are divided into two main categories: the average phase picking (APP) and the direct phase picking (DPP) [8]. The direct phase picking is simpler and faster, and it is typically used with higher data rates. For the scope of this paper

* Corresponding authors.
E-mail address: minagadelsayed@hotmail.com (M. Abdallah).

http://dx.doi.org/10.1016/j.mejo.2015.01.006
0026-2692/

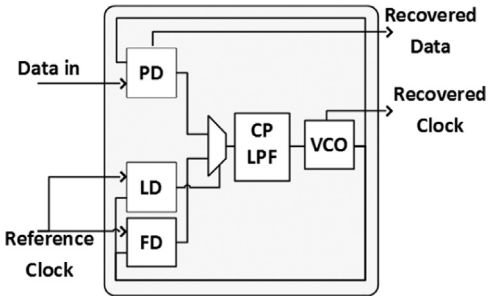

Fig. 1. Conventional PLL based CDR.

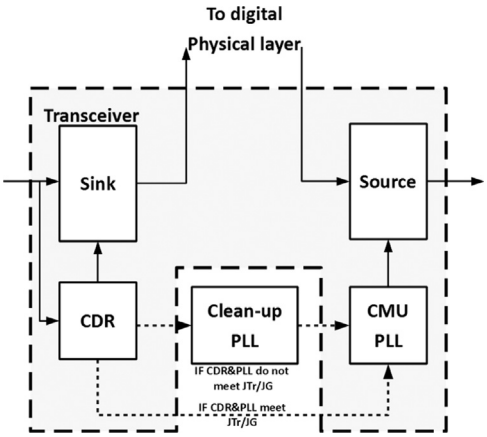

Fig. 2. Conventional PLL based CDR clocking scheme.

we are concerned with the DPP. The OSCDR architecture, similar to most digital architectures, is a feed-forward architecture; hence it is sometimes called blind over-sampling. The OSCDR suffers from a few disadvantages. The first is the lack of a recovered clock to be used for any further data transmission. The second is the poor tolerance for low frequency jitter and frequency error; this is a consequence of the lack of tracking between the sampling clock phase and the received data phase. Third is the relatively complex phase picking algorithms that limits the maximum achievable data rate. The semi-blind CDR (SBCDR) is a modified architecture derived from the OSCDR that addresses these disadvantages.

The SBCDR provides a phase tracking capability. The sampling clock is no longer a data independent internal clock, it is rather a recovered clock that tracks the received data phase. This provides low frequency jitter and frequency error tolerance [9]. The SBCDR loop is similar to a conventional phase tracking CDR such as phase locked loop CDR [6]. The exception is that the usage of the OSCDR as a phase detector within the SBCDR loop provides an extended jitter tolerance relative to both stand-alone OSCDR and conventional phase tracking CDRs. A simplified block diagram of the SBCDR architecture is shown in Fig. 3(a). The SBCDR still suffers from some of the disadvantages of both the OSCDR and the phase tracking CDRs. The OSCDR phase picking algorithm complexity can still limit the maximum achievable data rate. Within the phase tracking loop, the loop dynamics impose a strong trade-off between the three jitter metrics. The SBCDR extends the JTo without affecting either the JTr or the JG. However it still suffers from a strong trade-off, through the loop bandwidth, between JTr and JG. Another disadvantage, related to the phase tracking architecture, is the extensive use of analog and mixed-signal circuitry. This limits the ease of migration to newer technology as CMOS technology scales down.

The proposed SBCDR architecture utilizes a more digital intensive approach. The DAC/Filter/VCO combo is replaced by an all-digital phase locked loop ADPLL. This reduces the share of analog

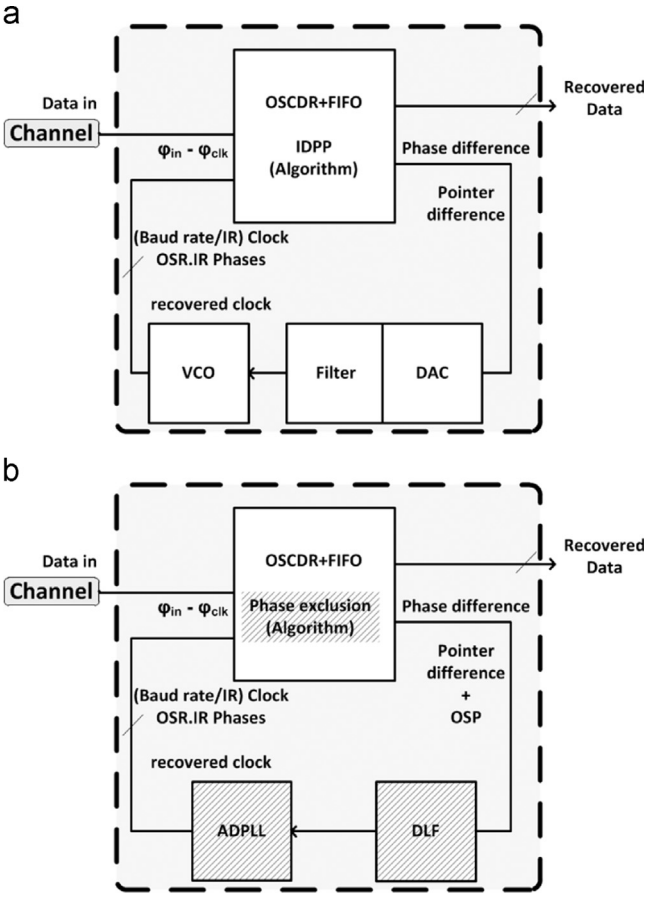

Fig. 3. (a) Conventional SBCDR architecture and (b) proposed SBCDR architecture.

circuitry in the system to only the digitally controlled oscillator (DCO) within the ADPLL. The ADPLL as well controls the JG of the CDR independent of JTR which is controlled through the main SBCDR loop.

Finally the DPP algorithm is replaced by a very simple phase exclusion algorithm. This new algorithm reduces all mathematical operation to NAND or NOR operations, and it also allows for pipelining in its implementation. This leads to a much higher achievable data rate.

3. Proposed architecture

A simplified block diagram showing the proposed modification in the SBCDR architecture is shown in Fig. 3(b). It should be noted that a digital loop filter (DLF) is used instead of an analog one as in the conventional SBCDR. A more detailed block diagram of the proposed design is shown in Fig. 4. The design is partitioned into three main macros. The OSCDR is based on the proposed phase exclusion algorithm. The ADPLL is the source of the recovered sampling clock. Finally the DLF closes the phase tracking loop. By disabling the DLF, the proposed CDR acts as a fully functional feed-forward OSCDR. Detailed architecture of these macros is described in the following sub-sections.

3.1. OSCDR

3.1.1. Architecture

The OSCDR architecture is based on the DPP algorithm. For a full rate operation this algorithm detects the data transition and picks the furthest sample as the recovered data. As the required