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A computationally efficient model of single electron transistor for analog IC simulation

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ABSTRACT

A compact analytical single electron transistor (SET) model is proposed. This model is based on the "orthodox theory" of single electron tunneling, valid for unlimited range of drain to source voltage, valid for single or multi-gate, symmetric or asymmetric devices and takes the background charge effect into account. This model is computationally efficient in comparison with existing models. SET characteristics produced by the proposed model have been verified against Monte Carlo simulator SIMON and show good agreement. This model has been implemented in HSPICE simulator through its Verilog-A interface to enable simulation with conventional MOS devices and single electron inverter has been simulated and verified with SIMON results. At high operating temperature, the thermionic current is taken into account.

1. Introduction

The single-electron transistor (SET) is one of the best candidates for future VLSI logic circuits because of its ultralow power dissipation, very small size, high switching speed and new functionalities [1–4]. It has unparalleled characteristics such as periodic increase and decrease of drain to source current with respect to gate voltage and increase of drain to source current as a function of drain voltage. Because of these unparalleled features of the SET in practical applications, analysis of its behavior in circuits is important. There are three techniques to simulate single electron transistor: the Monte Carlo (MC) technique, SPICE macro-modeling technique, and compact analytical modeling technique. MC technique is the most popular approach that is used to simulate single electron devices. It starts with all possible tunneling events, calculates their probabilities, and uses the probabilities for weighting [5]. Tunnel events are considered to be independent and exponentially distributed. The main part of an MC simulator is the random number generator. Several MC simulators (i.e., SIMON [6], KOSEC [7], SENECA [8], MOSES [9], SECS [10], and an adaptive algorithm SEMSIM [11]) are developed to model single electron systems. These models are the most accurate way to simulate SET, but they cannot be used for large-circuit simulation because they are extremely time consuming and cannot simulate hybrid SET/MOS circuits. In SPICE macro-modeling technique, SET behavior is modeled using equivalent circuits based on conventional microelectronic components (such as voltage and current sources, diodes, and resistors). Few research efforts on macro-modeling of SET have been reported [12–14]. In compact analytical modeling technique, the steady state master equation is solved to calculate drain to source current. Various analytical models have been proposed for SET [15–22], each of them based on the orthodox theory. All of them except the model introduced in [18] have operating drain to source voltage limitation. In this paper, an analytical model for SET has been proposed. This model is based on the orthodox theory of single electron tunneling, valid for unlimited range of drain to source voltage. In master equation approach, the simulation time is linearly dependent on the number of charge states. The proposed model includes the minimum number of states to capture certain values of drain to source voltage. So, it is less time consuming than other models while maintaining a good agreement with SIMON results. It is applicable for single or multi-gate devices and the background charge effect is taken into consideration. At high operating temperature, the contribution of thermionic current is included in the proposed model.

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2. Orthodox theory of single electron tunneling

The orthodox theory of single electron tunneling was first developed by Kulik and Shekhter [23] for a particular case study, and later it was extended by Averin and Likharev [1,24]. This theory is based on the following assumptions:

(1) Quantization of electronic energy inside the island is ignored; the electron energy spectrum is continuous. This assumption holds true for $E_c \gg K_B T$ (where E_c and $K_B T$ stand for charging energy and electron kinetic energy, respectively), otherwise thermal fluctuations in energy will overcome the single-electron charging energy, smearing out any single-electron effects.
(2) The time taken by the electron tunneling through the barrier is assumed to be negligible.
(3) Coherent quantum processes consisting of several simultaneous tunneling events, or co-tunneling, are ignored. This assumption is valid only when the electrons are well-localized in the island. To ensure localization, the tunneling resistance must be greater than the quantum resistance: $R_t \gg R_q = h/e^2 = 25.9\ K\Omega$.

3. Development of new model

3.1. Assumptions

Consider a metallic SET as shown in Fig. 1. The proposed model is developed on the following assumptions:

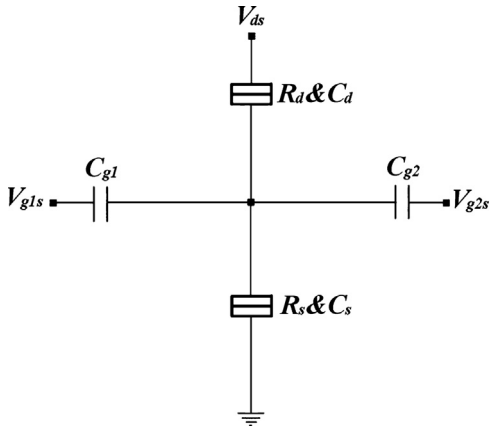

Fig. 1. Schematic diagram of a single electron transistor (SET).

- It obeys the orthodox theory of single-electron tunneling.
- The interconnect capacitances associated with the gate, source, and drain terminals are much larger than the device capacitances to ensure that the total capacitance of the island equals to the summation of all device capacitances, $C_\Sigma = C_d + C_s + C_{g1} + C_{g2}$.

3.2. Tunneling rates

An electron can only enter or exit the island by tunneling through drain or source tunnel junctions. The rate of electron tunneling through the tunnel junction is called tunneling rate, and is derived from Fermi's golden rule [1]:

$$\Gamma(\Delta G) = \frac{-\Delta G}{e^2 R_t\ (1-\exp((\Delta G/K_B T)))} \tag{1}$$

where ΔG is the difference between the final and initial Gibbs free energy of the system, R_t is the tunnel resistance of the junction, and T is the temperature. ΔG for each transition can be expressed as follows [5]:

$$\Delta G_{I\to D} = \frac{e}{C_\Sigma}\left[\frac{e}{2} - \left((C_s + C_{g1} + C_{g2})V_{ds} - C_{g1}V_{g1s} - C_{g2}V_{g2s} + q_0 + ne\right)\right] \tag{2}$$

$$\Delta G_{D\to I} = \frac{e}{C_\Sigma}\left[\frac{e}{2} + \left((C_s + C_{g1} + C_{g2})V_{ds} - C_{g1}V_{g1s} - C_{g2}V_{g2s} + q_0 + ne\right)\right] \tag{3}$$

$$\Delta G_{S\to I} = \frac{e}{C_\Sigma}\left[\frac{e}{2} - \left(C_d V_{ds} + C_{g1}V_{g1s} + C_{g2}V_{g2s} - q_0 - ne\right)\right] \tag{4}$$

$$\Delta G_{I\to S} = \frac{e}{C_\Sigma}\left[\frac{e}{2} + \left(C_d V_{ds} + C_{g1}V_{g1s} + C_{g2}V_{g2s} - q_0 - ne\right)\right] \tag{5}$$

where n is the net number of electrons in the island (or the number of charge states) and q_0 is the background charge.

3.3. Master equation

The orthodox theory provides the expression of one electron tunneling rate in a SET system, but it does not give any information about the statistics of many electrons tunneling [5]. If we assume that tunneling events have no memory and the states are discrete,

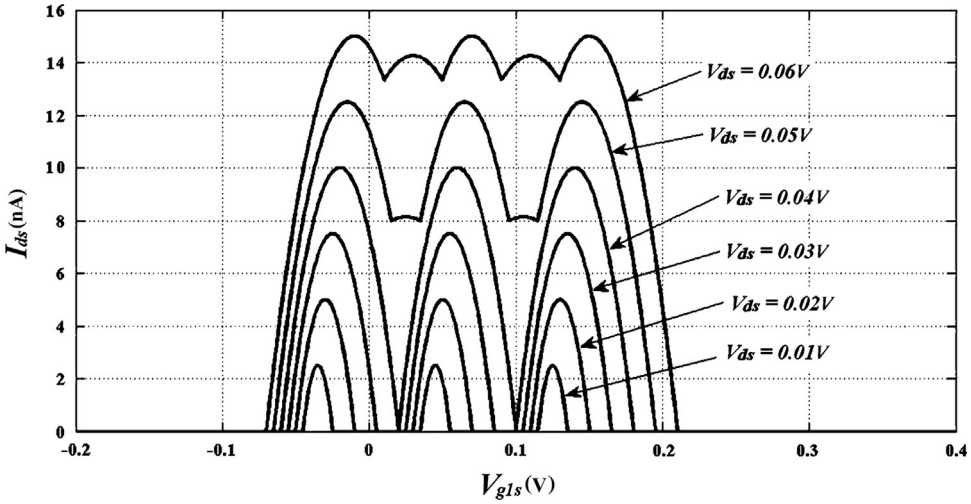

Fig. 2. $I_{ds} - V_{g1s}$ characteristics of a SET at $C_{g1} = 2$ aF, $C_d = C_s = 1$ aF, $C_{g2} = 0$ aF, $V_{g2s} = 0$ V, $T = 0$ K.