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Simulation and measurement of the capacitance benefit of air gap interconnects for advanced technology nodes

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ABSTRACT

Air gap (AG) interconnects, with an ideal dielectric constant *k* of 1, is a promising approach to reduce signal propagation delay. In this paper, a comparative study of AG and dielectric copper damascene interconnect structures is performed through Raphael™ electric field simulation to investigate the capacitance benefit of introducing AG when scaling to small dimensions. The variation in total capacitance as a function of half pitch is simulated for different AG integration schemes proposed in the literature. Ideal and practical cases of these different integration schemes are simulated and compared to assess whether interconnect structures using a low-*k* ($k = 2.3$) dielectric are more suitable than AG interconnects at scaled dimensions. The effect of using an additional (SiC-based) stiff liner on the AG capacitance benefit is also investigated. Finally, we verify our simulations using sub-40 nm half pitch AG structures prepared using the conformal and non-conformal processes.

1. Introduction

In the process of miniaturizing semiconductor devices, the interconnect dimensions are also downscaled. It has been commonly known that interconnect delay is the main limiting factor in the performance of ultra large scale integration (ULSI) integrated circuits [1]. This delay can be reduced by lowering the resistance R or the capacitance C of the interconnects. The capacitance reduction not only reduces the delay, but also reduces the cross-talk and power consumption, CV^2f for the same voltage V and frequency f. In order to reduce the interconnect capacitance, the dielectric constant value of inter-line dielectrics and inter-level dielectrics are reduced. New materials with k value less than 2.5 are being explored in the industry. The k value can be further reduced by introducing pores into the dense dielectric to form *porous low-k* materials [2]. When air, having the lowest possible k value of 1, is introduced into the dielectric materials, the effective k value of the dielectric material can be reduced to a great extent. However, as the degree of porosity in the porous low-k material increases, the integration challenges of these materials with copper metallization become increasingly severe. The difficulties include reduced mechanical robustness and vulnerability to damage during all stages of the Damascene process (etching, ashing, wet cleaning, barrier layer deposition and chemical mechanical polishing). Thus in the long run, an alternative solution is required.

A completely different approach is to use only air as the inter-line and inter-level dielectric material [3]. These kind of structures, which are targeted to use only air as the dielectric material, are called *Air Gap (AG)* structures. Currently, there are numerous methods to form AGs. They can be classified into two broad categories based on the steps followed [4]: (1) dielectric etch back combined with a non-conformal deposition or (2) decomposition of a sacrificial layer after subsequent cap layer deposition. However, the mechanical stability [5] and the electrical reliability [6] of these structures, using only air in between the interconnect metal lines, are not well established. As a result, some additional materials need to be introduced between the AG and metal structures. For example, in order to prevent the metal from being oxidized, a stiff thin layer of material, called liner, could be deposited on the sidewalls of the interconnects. In some processes, these are formed because of the non-ideal (conformal) formation of barrier layer [7]. These liner materials have negligible impact on the overall capacitance at larger dimensions [8]. However, at smaller dimensions, it can be expected to have greater impact and could be considered as a potential bottleneck. Hence, it is important to compare the capacitance scaling trend for AG structures with other low-k interconnect structures to find out the critical thickness and position of liner, at which the

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AG structures are advantageous. In this paper, we have analysed this through Raphael™ [9] electric field simulation, taking into account the different practical AG structures formed by different processes currently available in the literature. In literature, Raphael™ simulations were used only to calculate the effective dielectric constant for a particular method proposed in the same paper [7,10,11]. This will be the first paper to simulate the capacitance benefit for both the approaches to find out the optimal geometry of the materials in AG structures. Capacitance benefit is defined as the ratio of the difference between the capacitance of an air gap structure and that of a corresponding low-*k* structure, to the capacitance of the low-*k* structure.

In this paper, we first explained the different AG structures that were simulated, their dimension rules and the motivation behind their geometry by referring to previous literature. The Raphael™ simulation results are then reported; discussed and compared with the results of the capacitance measurement. For the measurement, two different experimental copper AG interconnect structures were fabricated together with a reference copper porous low-*k* interconnect to verify the simulation results. We conclude the paper by summarising the important results in relation to applications of the AG processes.

2. Simulation

We have simulated the possible outcome of capacitance with scaling for the different methods proposed in the literature for the formation of AG. According to the 2011 International Technology Roadmap for Semiconductors (ITRS), AGs are projected as a solution to achieve effective *k* values of less than 2.0 for the 16 nm technology node and beyond as materials improvements become increasingly difficult [12]. Ideally, only air should be present in between the interconnect metal lines. Even though there are different AG integration schemes available in the industry, based on the way AG structures are formed, there are only two basic approaches to form an AG [4]. The first approach involves deposition of dielectric in between the interconnect metal, followed by etch back of the dielectric and a non-conformal cap layer deposition. Although this method is expected to form only an AG between the interconnect lines, the cap layer material can be deposited also on the sidewalls of the lines [7,13]. The material forms an inverted 'V' shaped structure above the AG, which is called *Projection* in this paper. The main limitation of the Non-conformal deposition method is that it is difficult to achieve AGs by pinch-off in dielectric regions with smaller aspect ratios (defined as the ratio of height to width). Typically, an extra lithographic step is required to define those dielectric areas where AGs can be introduced and this increases the process cost.

The second approach for AG formation starts with the deposition of a decomposable material called *sacrificial layer* in between the interconnect lines. After the cap layer deposition, the sacrificial layer is removed either by etching [14] or by thermal decomposition [10]. In this approach, there is also no ideal formation of only AG between the interconnect lines. A thin layer of sacrificial material is left undisturbed on the sidewalls of the lines [14,10]. In some of the AG schemes proposed in the literature, an additional stiff liner is added purposely on the sidewalls of the lines by conformal deposition to improve mechanical and electrical reliability [4,6] and prevent metallic damage [7,14,15] during etch back. Hence, the effect of this (SiC based) liner, on the AG capacitance benefit is also investigated. Although trenches with wide AGs can be fabricated using the Sacrificial layer method, the resulting wide spaces, can lead to poor mechanical integrity [16]. Another challenge with these two approaches and especially the Non-conformal method is the unlanded via. This is an integration issue that can arise as a result of misalignment during via lithography. An unlanded via could lead to via metal intrusion into the AGs and result in reliability problems even at the 32 nm technology node [17]. Irrespective of the approach used, compared to the low-*k* dielectric structures, AG structures will incur higher manufacturing costs as the number of process steps is increased [16].

Simulations were performed using a 2D static field solver, Raphael™. The model is built using code by Raphael™ software and the various cases are executed by interfacing it with Optimus® software. Fig. 1 shows the different AG interconnect structures that are simulated. The optimal structure obtained by the Sacrificial layer decomposition approach is represented as *Ideal* structure (Fig. 1a) and the *Side-Liner* structure (Fig. 1b) [15] and *All-Liner* structure (Fig. 1c) [18] represent the practical implementations of the approach. *Non-Conformal* structure (Fig. 1d) represents the optimal structure obtained for dielectric etch back approach and practical implementation of this approach [7] is represented by the *Conformal* structure (Fig. 1e). *Non-Conformal* is different from *Ideal* by the projection of the cap layer. *Side-Liner*, *Conformal* and *All-Liner* have a liner material on the sides of the metal to improve the mechanical stability of interconnects. *All-Liner* has an extra liner between adjacent interconnect lines at the bottom of the air gap. Additionally, *Conformal* has a projection of the cap layer. The default structure has AG at metal 2 (M2) only. The interlevel dielectric has $k = 2.3$ at the M1 level and M3 level. Depending on application, the AG may be required to extend below to vias and above the copper metal level M2. Hence, these variations are also considered for each case. The values assumed for different parameters and scaling rules are shown in Table 1.

3. Experiment

In order to verify the applicability of the electric field simulations to practical implementation of AG structures, three kinds of single damascene interconnect test structures with a 40 nm half pitch were fabricated. For each test structure, the line length and height were 1 cm and 100 nm respectively. One reference test structure was fabricated with low-*k* material with $k = 2.3$. The other two AG samples prepared represent the *Non-Conformal* process by dielectric etch back and the *Ideal* process by sacrificial layer decomposition. All the single-damascene test structures were fabricated using a similar process but the AG formed at different stages. A dual hardmask of 25 nm SiO_2/30 nm SiCN was used to protect the 100 nm dielectric. Lithography for this work was carried out on an ASML Alpha Demo Tool. A 20 nm organic under layer (UL) was used to minimise out gassing and promote adhesion of the 80 nm EUV photo-resist. Separate etch chemistries were developed for UL, SiO_2, and SiCN hardmask opening. After trench etch metallization consisting of a 1.5 nm TaTaN physical vapour deposition (PVD) barrier layer with a 20 nm Cu seed was deposited. Trenches were filled with electrochemical-plated (ECP) Cu. Finally, 30 nm SiCN/SiCO, 500 nm Si_3N_4 and 300 nm SiO_2 were deposited with Al contact pads to complete the passivation stack. In the case of the *non-conformal* approach, the dielectric was decomposed prior to capping and the non-conformal nature of the SiCN/SiCO could create the AG. To create the *ideal* case, the dielectric was decomposed at high temperature after passivation. The parasitic capacitance per unit length of each test structure was measured for multiple samples and the capacitance benefit was determined directly from these measurements.

4. Results and discussion

Fig. 2 shows the capacitance benefit as a function of half pitch (10–100 nm) for the five different integration schemes. For each