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Reliability enhancements of chip-on-chip package with layout designs of microbumps

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ABSTRACT

To enhance the assembly quality and mechanical reliability of microbumps during the stacking process of multiple thin chips and during temperature cycling tests, a novel wafer-level underfill (WLUF) fabrication technique has been proposed to resolve these problems. However, the occurrence of a severely warped condition or gap reduction between stacked chips has been observed during WLUF assembly with thermal compression. This condition prevents the objective achievement of a three-dimensional integrated circuit package. To address such an urgent issue, this study presents process-oriented stress simulation based on the finite element method to determine its root cause. Using a comparison with experimental data, results indicate that the major influential factors inducing thermomechanical stress within a chip-on-chip package are caused by a large temperature difference in the mechanical properties and process of WLUF. The use of WLUF with a low coefficient of thermal expansion and a low Young's modulus is beneficial because it reduces plastic strain of critical microbumps. The use of layout designs for microbump arrays with arranged dummy joints significantly improves the co-planarity of the whole packaging structure. The simulated predictions indicate that when more than three dummy joints are placed near the outermost microbump, the warping variation between the packaging center and the chip edge at the top surface of a package under a load of a 2.0 kg bonding force would be <70 nm. Simultaneously, a minimum equivalent plastic strain of ~0.87% on the critical microbump is obtained during a thermal cycling load.

1. Introduction

Three-dimensional (3D) integrated circuit (IC) packaging has been given much attention because it possesses several advantages over the traditional packaging technology, such as its high interconnect density, superior form factor, the integration of heterogeneous functions, and desirable performance [1]. Multi-chip stacking with a thinning procedure is generally implemented using simultaneous Cu–Cu or Cu–Sn thermocompression and adhesive buffer layer bonding [2]. However, this approach is still at the infancy stage and must be further developed to meet the reliability requirements and corresponding yields of the microelectronic industry. Consequently, the promising flip chip bonding process combined with the architecture of through-silicon via (TSV) is widely utilized in chip-to-chip interconnects of 3D integrations [3–4]. Meanwhile, numerous critical reliability issues regarding the effects of TSVs and microbumps on thermal dissipation [5], joule heating, electromigration, stress-migration, cracking failure, and the structural warping of a stacked chips assembly [6–7] have become severely challenging and require urgent resolution [8]. The energy-partitioning and Coffin–Manson approaches integrated with the finite element analysis (FEA) are suggested to estimate the thermomechanical reliability of microbumps using the mean failure time of microjoints and TSVs, respectively [9]. The mechanical properties of filled underfill and bump height are the most dominant factors that influence the reliability of 3D-IC packaging with stacked four chips. The locations of microbump-adjacent chips with a high magnitude of inelastic strain have become a particular concern caused by the large coefficient of thermal expansion (CTE) that occurs at this condition. Without the underfill, the measured shear strengths of bonded chips and microbumps exceed the demand specifications [10]. Compared with the dimensional orders of flip chip solder bumps, the microbumps dramatically decrease, which significantly induces the Ag_3Sn production of intermetallic compounds (IMCs) as Pb-free SnAg solders are adopted. Interfacial cracks may be initiated and could grow at the locations of IMCs because 3D-IC packaging is subject to external stress [11]. To change the thermal stress distribution of bonding interface of microbumps and increase crack resistance,

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several Cu pillar bump types were examined by FEA [12]. The optimization of microbump layouts could be further performed to enhance the reliability of analytic 3D-IC packaging structures [13].

A review of the literature revealed that the use of underfill is necessary to improve the lifetime of microbumps. Consequently, a wafer-level underfill (WLUF) technique was presented to overcome the drawbacks of capillary actions used in the traditional underfill processes for a narrow bump gap [14–15]. However, the issue of warping during the WLUF process influences the subsequent assembly of chip stacking and the mechanical reliability of microbumps. To investigate this concern, a vehicle for the chip-on-chip packaging structure (Fig. 1) is utilized to understand the warping induced by chip stacking. Using four microbump arrays combined with the WLUF process, a 5.1 mm × 5.1 mm top chip is assembled onto a 16 mm × 16 mm bottom chip. The detailed sizes of microbumps with a fine pitch of 30 μm are likewise revealed in Fig. 1(b). The cross-sectional views of microbumps under different magnitudes of bonding forces are shown in Fig. 2. The gap reduction between chips at the edge is extremely serious, as compared with the packaging center. To estimate the warping in the WLUF assembly and the mechanical reliability of a critical microbump during a temperature cycling period, a nonlinear simulation method is proposed in this study; the method is based on FEA integrated with process-oriented considerations. Furthermore, to address the issue of warping, two different layout designs for microbumps with dummy joints are systematically analyzed. These structural designs ensure the mechanical reliability of a WLUF technique.

2. Theory of thermal stress

The major driving force of structural failure caused by thermal stress has been a long-term concern for electronic devices. This observation is particularly true because thermal stress has an important influence on the reliability of 3D-IC packages. The sources of thermal stress could be grouped into two: (1) a temperature gradient distributed around a single material such as the operated condition of a silicon chip; and (2) the assembly of materials at the bonding interface with different thermal extensions under the thermal cycling load or the temperature of the fabrication process. Usually, these phenomenons can be observed during tests of electronic packages and the film deposition of IC chips. In this study, a simulated analysis based on the finite element method (FEM) is assumed to be a steady-state process because cases of heat source and heat transfer have not been observed. Conse-

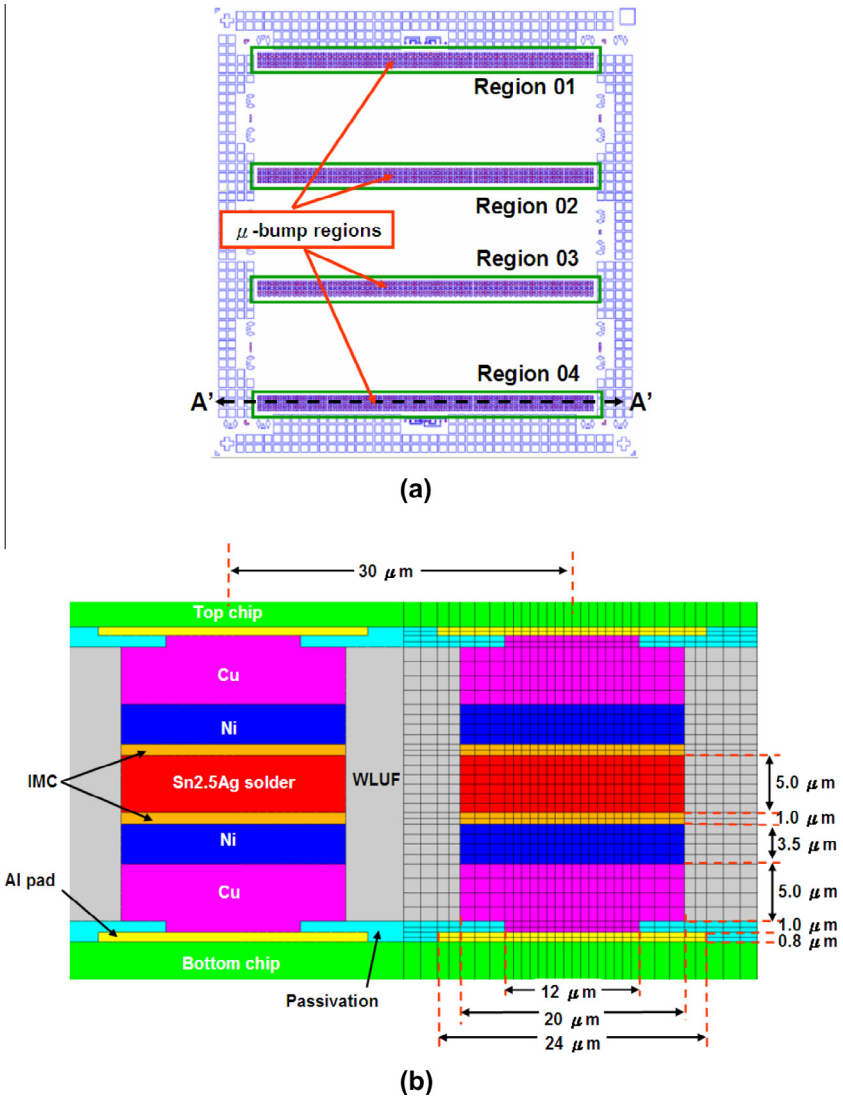

Fig. 1. Schematic of the packaging framework: (a) layout of microbump regions in chip-on chip packaging; (b) cross-sectional view and related dimensions of microbump arrays.