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Ni(Pt) silicide with improved thermal stability for application in DRAM periphery and replacement metal gate devices

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ABSTRACT

In comparison to standard CMOS devices for logic applications, periphery devices for DRAMs typically require a long anneal in the temperature range between 600 and 800 °C after the silicide formation. This gives additional constraints in many process steps, in particular in the silicidation step. In this work the feasibility and optimization of a thermally stable NiPt silicide has been investigated. First, a blanket wafer study has been done showing that a thermally stable silicide (TSS) can be obtained by using a pre-amorphization implant (PAI) + C implant + laser anneal prior to the silicidation process, and a superior thermal stability can be obtained using a spike anneal rather than a laser anneal. Then, this silicide was successfully integrated in low voltage CMOS HKMG devices (Lgate down to 32 nm) without affecting the junction behavior, and featuring only minor effects on devices performance compared to a non-stabilized NiPt silicide without DRAM anneal, with applicability in a replacement metal gate process flow.

1. Introduction

Silicides have been used in self-aligned processes for several generations of CMOS devices, with the aim of reducing the sheet resistance and providing stable Ohmic contacts with low contact resistance on gate, source and drain areas. One of the major differences between DRAM periphery and logic devices is that the former typically have to sustain long, moderate to high temperature anneals after the transistor fabrication [1]. These anneals are required for the DRAM cell fabrication and for the related Back End process and in the following will be called DRAM anneals (DA) [2–4]. To keep up with scaling, DRAM periphery transistors will adopt features of logic devices such as high-K dielectrics and metal gates (HKMG) for better performance, lower power consumption and improved external resistance [2]. With the implementation of metal gates, the sheet resistance of the gates is fully decoupled from the silicidation process, widening the choice of materials and optimization options for this process step.

The reduced access resistance can be achieved by replacing the silicidation through contact holes by complete silicidation of the source/drain areas as is common practice for logic devices [1]. The Ni(Pt) silicide typically used suffers from too limited thermal stability to sustain the high thermal budgets needed for manufacturing of the DRAM devices [5].

It has been demonstrated that addition of Carbon (C) to the Silicon (Si) substrate improves the thermal stability of the formed NiPtSi [1,5–12]. The C can be incorporated by deposition of epitaxial Si:C [7,9] or by C implantation in the Si junction areas [1,9,10]. On the one hand it has been demonstrated that the thermal stability increases with the implanted C dose [11], but on the other hand the NMOS V_T-*Lg* roll-off and PMOS device performance are degraded [13].

This work will focus on the optimization of the thermally stabilized NiPt silicide with special attention to the effect of the nature (laser vs. spike) and temperature of the post C implant anneal and the influence of the presence and nature of the pre-amorphization implant (PAI). After a study on blanket wafers, the thermally stable silicide has been successfully implemented in a CMOS HKMG flow, with Lgate down to 32 nm.

2. Materials and methods

All thermally stable silicide samples used in this study are based on NiPt silicide using the (PAI), the C implant and the anneal silicide stabilization steps. The process evaluated consists of a PAI of the N+ and P+ source/drain (S/D) implanted areas, followed by a C implant and extra anneal. Afterwards a NiPt silicide is formed using a 10 nm initial NiPt layer. The Pt concentration was determined as less than 5% by Rutherford backscattering spectrometry. The process parameters varied are: (a) the presence and nature of the PAI, with no PAI, Germanium (Ge) PAI and Fluorine (F) PAI, (b)

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the implanted C dose, and (c) the temperature and type (spike or laser) of anneal if a post C implant anneal is used.

After the initial silicide formation, different anneals were applied consecutively on the same wafers: 600 °C 4 h, 650 °C 30 min, 675 °C 30 min or 700 °C 30 min DRAM anneals. After each thermal step, the thermal stability of the stabilized NiPt silicide was evaluated (i) by measuring the evolution of the sheet resistance and (ii) by top down SEM inspections to characterize the morphology of the silicide films.

Fig. 1 (*left*) shows a sketch of the 4-point sheet resistance measurement line scan performed on each wafer. The silicides were fabricated on 300 mm blanket wafers with representative N+ and P +S/D implants and activation anneal (1035 °C spike). The evolution of the sheet resistance with the additional thermal treatments applied is shown in Fig. 1 (*right*).

The thermally stable silicide was also implemented on CMOS device lots, presented in Section 4. An HKMG CMOS flow based on metal inserted poly silicon (MIPS) with Lgate down to 32 nm, realized in the 300 mm imec facility has been used [3]. To simulate the effect of the DRAM process on the gate stack and the silicide, a 600 °C 4 h DRAM anneal is either applied immediately after the junction anneal (before silicidation) or after the pre metal dielectric (PMD) chemical–mechanical polish (CMP) (when the silicide is in place).

3. Blanket wafer results

Fig. 2 shows the median and the standard deviation of sheet resistance measured on N+ (*top*) and P+ (*bottom*) S/D regions of the as-formed NiPt silicide and their evolution with subsequent DRAM anneals. Each column summarizes the evolution with the additional applied DRAM anneals, as in Fig. 1 (*right*), for the different silicides considered. An increase in the sheet resistance and/or its distribution is a sign of silicide degradation by transformation to a more resistive phase or indicates agglomeration. For the N+ case, a C implanted sample (4 KeV, 2e15at·cm^{-2}) without PAI and post anneal is included for reference. This features good thermal stability for a 600 °C 4 h DRAM anneal but degrades for higher DRAM anneal temperatures, as shown by the fact that the median is out of scale in the considered range. Adding the PAI and the post C implant anneal results in silicide stability up to 700 °C for the same C dose. This confirms that a PAI of Si prior to the C implant is required for improved thermal stability. As suggested in [10], C has to be incorporated into the re-crystallized Si to obtain improved thermal stability. Fig. 2 also illustrates that for both N+ and P+ Si, where a Ge PAI (12 KeV, 1e15at·cm^{-2}) and a post C implant laser anneal are used, improved thermal stability is obtained for the higher C doses (3.5e15at·cm^{-2}). This improved thermal stability is obtained at the expense of increased initial silicide resistance. This can be explained by an increase of the onset temperature of the silicidation reaction accompanied by an increased agglomeration temperature of the NiPtSi, as observed for NiSi with epitaxial Si:C [3].

For P+ active regions and Ge PAI, a superior thermal stability can be obtained at lower C doses (1e15at·cm^{-2}) if a spike anneal is used instead of a laser anneal. A medium C dose (2e15at·cm^{-2}) with >950 °C spike anneal allows to reach the same thermal stability than high C dose (3.5e15at·cm^{-2}) and laser anneal. This has the advantage to reduce interferences with dopant atoms (e.g. boron (B) diffusion as reported in [1]). On N+ active regions with Ge PAI, a medium C dose (2e15at·cm^{-2}) is sufficient to obtain high thermal stability with both spike and laser anneals.

Concerning the Ge PAI with spike anneal, the optimal spike anneal temperature for improved thermal stability differs for N+ and P+ active regions. Lower (900 °C) and higher (1035 °C) anneal temperatures are optimal for NMOS and PMOS devices, respectively, though both offer a sufficiently good thermal stability to the silicide. In the N+ case, when the spike anneal temperature increases, two different trends are observed: the sheet resistance of the as formed silicide decreases (blue line), while the sheet resistance of the 700 °C 30 min DRAM anneal increases (red line). This indicates that the onset temperature of silicidation and agglomeration decreases with the increase of the spike anneal temperature. However, the data suggest that the NiPt silicides stabilizes on N+ above 700 °C. For P+ regions, the sheet resistance of both as formed silicide and 700 °C 30 min DRAM anneal decrease with higher spike anneal temperature. It has been shown also that Ge PAI and post C implant laser anneal are thermally stable up to 750 °C [13]. Therefore, we can conclude that the thermal stability of NiPt silicide on P+ regions is expected to be above 750 °C, while for N+ regions it is expected to be about 700 °C. A slightly improved thermal stability of the NiPt silicide for N+ and P+ active regions is observed with F PAI (10 KeV, 2e15at·cm^{-2}) as compared to Ge PAI.

Fig. 3 shows a selection of SEM images taken to verify the integrity of the silicide after DRAM anneal. They show the thermally stabilized NiPt silicide, obtained by using 10 nm NiPt, Ge PAI + medium carbon concentration implant (2e15at·cm^{-2}) + 1035 °C spike anneal, for the N+ and P+ active regions, after 600 °C 4 h and 650 °C 30 min DRAM anneals. The integrity of the silicide up to 600 °C is

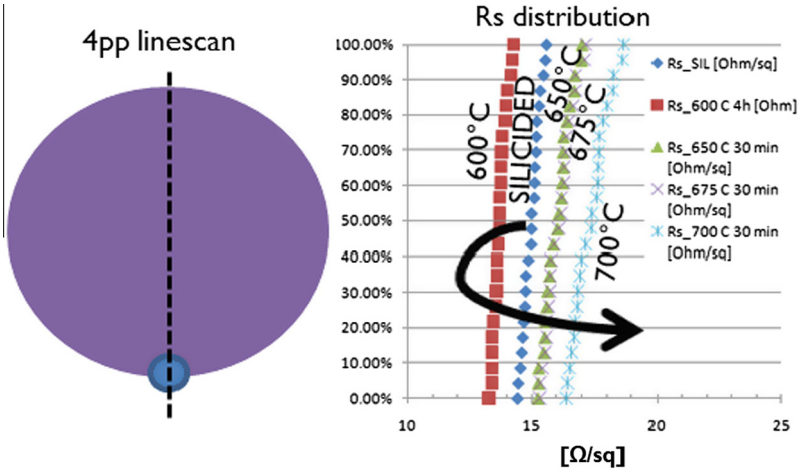

Fig. 1. (*left*) Sketch of line scan used for the 4-point sheet resistance measurement. (*right*) Evolution of the cumulative distribution for sheet resistance with the additional thermal treatments. In the presented case, the evolution of both median and spread with the temperature of the anneals is clearly visible.