Microelectronic Engineering 120 (2014) 210–215

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Carbon nanotube based via interconnects: Performance estimation based on the resistance of individual carbon nanotubes

Holger Fiedler [a,*], Marius Toader [b], Sascha Hermann [a], Raul D. Rodriguez [c], Evgeniya Sheremet [c], Michael Rennau [a], Steffen Schulze [b], Thomas Waechtler [a,d], Michael Hietschold [b], Dietrich R.T. Zahn [c], Stefan E. Schulz [a,d], Thomas Gessner [a,d]

[a] Chemnitz University of Technology, Center for Microtechnologies (ZFM), 09126 Chemnitz, Germany
[b] Chemnitz University of Technology, Institute of Physics, Solid Surface Analysis, 09107 Chemnitz, Germany
[c] Chemnitz University of Technology, Institute of Physics, Semiconductor Physics, 09107 Chemnitz, Germany
[d] Fraunhofer Institute for Electronic Nano Systems (ENAS), 09126 Chemnitz, Germany

ARTICLE INFO

Article history:
Available online 23 July 2013

Keywords:
Carbon nanotube
Interconnect
Post CNT growth process
Electrical characterization
Atomic force microscopy
Raman spectroscopy

ABSTRACT

Carbon nanotube (CNT) based interconnects with an improved bottom metallization scheme were prepared and characterized. Two procedures are introduced to enhance the CNT via performance after planarization. Both, temperature annealing of the metal-CNT contact and exposing the CNT tips to HF vapor prior to the deposition of the top metallization increased the yield and reduced the resistance of the vias. For a via of 5 μm diameter and a depth of 800 nm a resistance of 8 Ω was obtained.

Further, the resistance of individual CNTs was measured by means of conductive atomic force microscopy (cAFM), giving a value of 38 kΩ/CNT. We highlight the capability of cAFM to accurately predict the overall electrical performance of CNT based vias.

Deviations of the measured resistance compared to the theoretical limit are either attributed to defects in the CNT's atomic structure or imperfect contacts. To separate those two aspects, different methods to investigate the microstructure of the employed materials were used.

1. Introduction

In the state-of-the-art interconnect scheme of ULSI devices, Cu is employed as wiring material. However, the continuous down scaling in microelectronics causes detrimental size effects in the interconnect system. Among others, those lead to tremendously increasing resistance values and hence dramatic increase in heat dissipation. As a potential solution to address those issues, carbon nanotubes (CNTs) were proposed in the International Technology Roadmap for Semiconductors [1]. CNTs have several advantages compared to Cu, like a strong resistance towards electromigration [2] and a large electron mean free path [3], as well as a high thermal conductance [4–6].

Currently, the focus of the CNT based interconnects research lies on the vertical connections (vias) [7–12]. To outperform Cu interconnects, several difficulties have to be overcome, like a sufficiently high CNT density [13–15], a high CNT quality [16,17] and a low contact resistance [18,19]. Further, the integration scheme to incorporate CNTs has to be compatible with the established BEOL integration scheme. This concerns the thermal budget for CNT growth [20] and the interface to established Cu based interconnects [10]. Some reports about CNT based vias incorporate Cu in the bottom metallization [9,10,20,21], already.

Here, we address the formation of the CNT-metal contact at the top and the bottom metallization of the via. After incorporating a suitable diffusion barrier, which is less prone to oxidation than a pure metal, we use a measurement scheme designed to evaluate the CNT integration process. The usage of conductive atomic force microscopy (cAFM) to investigate CNTs is sometimes employed [22–24]. However, reports about the electrical performance of individual CNTs incorporated into via structures are rare [25]. Here we highlight that, once a reliable bottom metallization is achieved, cAFM can be used to accurately predict the electrical via performance. In conjunction, the CNT quality and the metal-CNT contact is investigated by Raman spectroscopy and imaging, transmission electron microscopy (TEM) and scanning electron microscopy (SEM) to reveal the mechanisms behind different contact optimization procedures.

2. Experimental

The process flow for the integration of CNTs into vias is shown in Fig. 1.

* Corresponding author. Tel.: +49 371 531 38572; fax: +49 371 531 8 38572.
E-mail address: holger.fiedler@zfm.tu-chemnitz.de (H. Fiedler).

0167-9317/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2013.07.007

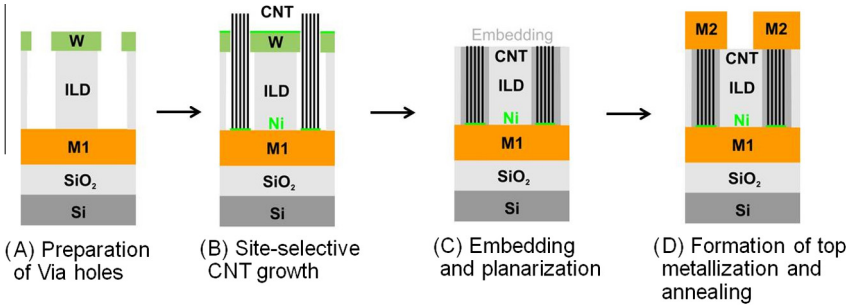

Fig. 1. Scheme for the integration of CNTs in vias.

The bottom metallization (M1) is sputter deposited without vacuum break, consisting (from bottom to top) of a 10 nm Ta / 20 nm TaN /100 nm Cu /20 nm TaN /10 nm TiN layer stack. The interlayer dielectric (ILD) with a thickness of 800 nm is composed of silicon oxide prepared by plasma-enhanced chemical vapor deposition. After the deposition of a 25 nm thick tungsten layer, conventional photolithography is applied to define the vias. Subsequently, the tungsten and the main part of the ILD are patterned by reactive ion etching. The last 100 nm of the ILD are removed by wet chemistry. For this purpose a buffered aqueous solution, based on a 1:5 mixture of $HF_{40\%}$ and $NH_4F_{40\%}$, has been applied. Afterwards a 2.3 nm Ni catalyst layer is deposited by electron-beam evaporation. CNTs are grown by thermal chemical vapor deposition using ethene, with a purity of 99.9999%, as carbon precursor. The process lasts for 10 min and is performed at a temperature of 600 °C. Further details about the CNT growth process can be found elsewhere [26]. Afterwards the CNTs are embedded in SiO_2 using the decomposition of tetraethylorthosilicate (TEOS) in the presence of ozone, followed by the planarization of the CNT vias by means of chemical mechanical planarization (CMP). If an HF treatment is applied, wafers are exposed to HF vapor for 20 s before the deposition of the top metallization M2. For the M2 layer stack, first, a 50 nm thick Ta layer is sputtered to contact the CNTs. Without breaking the vacuum, 10 nm TaN and 500 nm Cu are deposited on top of the Ta. Photolithography, wet etching of copper, and reactive ion etching of the Ta-based layer are used to pattern the structure. Finally, the wafer is temperature annealed for 30 min at 450 °C in a forming gas N_2:H_2 (5:1) atmosphere.

Considering the process flow, the cAFM and Raman investigations were performed on planarized samples, prior to the deposition of the top contact. Raman spectroscopy and cAFM measurements were carried out on the same sample, while a different wafer, subjected to the same process flow, was used for the electrical characterization of the via structures.

cAFM was performed on the sample to probe the variation of the CNT conductance within an array of vias. All data were recorded using a 5500 AFM from Agilent Technologies using a Ti/Pt coated AFM probe (tip radius <40 nm) with a spring constant of ~0.12 N/m. The simultaneously obtained topography and current mapping images were both recorded in contact mode. Each *I–V* set shown within this work is an average of 10 spectra recorded at the same contact point. 100 points within the indicated voltage range and 2 s acquisition time were used per individual spectrum. Since the maximum current that can be measured with the system is 10 nA, a resistor of 1001 kΩ was introduced into the setup. This resistance value is subtracted from the measured value to obtain the resistance of a single CNT.

Raman measurements were performed in the backscattering geometry and in the spectral range (1200–2800)cm^{-1} using the 514.5 nm wavelength of an Ar^+ laser and a Renishaw LabRam HR800 spectrometer integrated with an optical microscope with a 100× objective (N.A. 0.9) giving a diffraction limited resolution of $\lambda/(2\,N.A.) \approx 286$ nm. The laser power was limited to the range (0.5…2)mW in order to prevent sample damage. For statistical characterization of sample homogeneity, a region ($25 \times 25\ \mu m^2$), containing 25 vias with a diameter of 2 μm, was scanned and full Raman spectra were acquired with a step size of 500 nm.

The scanning electron microscope (SEM) images were obtained on a ZEISS Auriga 60 CrossBeam Workstation. With the same tool, cross-sections for high-resolution transmission electron microscopy (TEM) were prepared using the focussed ion beam (FIB) technique. The TEM lamellae were cut using focussed Ga ion beams down to 10 pA with an energy of 30 keV. For the lift-out of the lamellae, a Kleindiek MM3A micromanipulator, installed on the Auriga 60, was used. With the manipulator, the lamellae were transferred to Cu lift-out grids and attached by ion-beam assisted, in situ Pt deposition.

High-resolution TEM (HRTEM) was performed using a Philips CM 20 FEG equipped with an imaging energy filter from Gatan which allows electron energy loss spectroscopy (EELS) to be performed. Energy-filtered TEM (EFTEM) images can be obtained through EELS elemental mappings.

The electrical characterization of vias was carried out on an automatic probing station (Cascade PA200) equipped with a Keithley 4200SCS current source. Each resistance value is based on the slope of an *I–V* curve obtained in the voltage range from −100 to 100 mV. If the regression coefficient of the linear fit is smaller than 0.8, we consider the respective via structure to have failed.

3. Results and discussion

3.1. Electrical characterization of individual CNTs by cAFM

Within the investigated region a very homogeneous distribution of the conductance map was observed (Fig. 2). In contrast to a solely Ta based bottom metallization [26], no major differences between individual vias were found with the current bottom metallization scheme that involves TiN as the uppermost material before CNT growth.

Taking into account the CNT density ρ of $(2.1 \pm 0.3)^{*}10^{10}$ CNT/cm^2 and the guaranteed AFM tip radius r_{AFM} to be below 40 nm, the number N of CNTs in contact to the AFM tip can be estimated using Eq. (1).

$$N = \rho\, \pi\, r_{AFM}^2 \tag{1}$$

Numerically, N is calculated to have a value of (1.05 ± 0.15). Hence, we assume that the measured resistance is characteristic for a single MWCNT.

The electrical properties of individual MWCNTs were determined at two stages. Directly after planarization a resistance of (66 ± 17)kΩ/CNT was obtained. In contrast, after HF exposure, the CNTs in the same vias exhibit a reduced resistance of (38 ± 12)kΩ/CNT.