# Electrochemical fabrication of platinum interconnects for implantable electronic devices

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## ARTICLE INFO

## ABSTRACT

In this paper we report on fabrication of Platinum (Pt) interconnects on the flexible bio-compatible substrates, having in mind possible applications in implantable medical devices. We aim to replace physical vapor deposition methods (PVD) with plating in cases when this is cost effective, i.e. when only a small fraction of the substrate needs to be coated with Pt. We optimize plating parameters by doing tests on coupons, and then explore up-scaling the process to 2 inch wafers and larger substrates/carriers covered with releasable polyimide layers. Physical and chemical properties of deposited lines are assessed, and post-plating steps developed so that characteristics of electrochemically deposited (ECD) Pt match those of PVD Pt.

## 1. Introduction

Platinum (Pt) is widely used for fabrication of electrodes and interconnects in bio-medical electronic devices [1–3] due to its biocompatibility, corrosion resistance and good electrical conductivity. Its main drawback is that is very expensive, requiring careful design considerations in order to keep fabrication costs under control. In the case of interconnects, when large portions of the substrate being deposited on are not covered by Pt, electrochemical deposition (ECD) techniques could offer significant cost-savings over commonly used physical vapor deposition (PVD) methods [4]. Successful implementation of Pt plating on large, wafer scale substrates, in a fashion similar to fabrication of copper (Cu) interconnects for needs of microelectronics industry, could further reduce the production costs. Studies of Pt electrodeposition on biocompatible substrates have been published in scientific literature in the past [6–10], but they are typically performed on small coupon scale and under potential control. This is understandable since both smaller sample size and potential control allow easier analysis of Pt plating phenomena. However, most commercial plating tools (to our knowledge) use constant current deposition mode, and it is not a priori clear whether, and how, this would affect the quality of the deposit. Of course, there are also requirements regarding uniformity of the plated structures across the large substrate area, and reproducibility and stability of the deposition processing steps. And, these are not the only challenges. To reduce risks of pronounced foreign-body-reaction (FBR), infection and irritation, novel implantable devices have small, soft, and comfortable packaging [1,2]. Thus, Pt lines must also be mechanically sound enough to withstand bending, stretching and other motion of the packaging, allowing continuous functioning of the implanted devices.

In this work, we explore the possibility to fabricate Pt interconnects on flexible biocompatible substrates using ECD methods. Since ECD requires conductive substrates, all samples are seeded with PVD TiN. We study fundamentals of galvanostatic (constant current) deposition of Pt on coupons, and optimize plating parameters for transfer to 2 inch wafers and larger substrates coated with flexible and biocompatible polyimide layers. The use of Silicon (Si) or glass substrates enables easier manipulation and transport of the samples, but in the end, flexible polyimide layers with Pt interconnects are to be released from the carriers and serve as stand-alone entities. We examine properties of deposited lines using techniques such as scanning electron microscopy (SEM), X-ray diffraction (XRD), atomic force microscopy (AFM), and 4-point probes, and, if necessary, develop post-plating processing steps resulting in ECD Pt closely matching PVD Pt characteristics. Based on the level of success of these experiments, we discuss the potential use of ECD Pt in flexible implantable medical devices, and perspectives for further up-scaling to wafer-level processing.

## 2. Materials and methods

Initial studies of Pt film electrochemical deposition were performed on blanket PVD TiN/Si wafer coupons using 36 mM

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dihydrogendinitrosulfatoplatinate(II) (Alfa Aesar) plating bath. Plating experiments were performed using a three-electrode clip-on Teflon cell connected to a computer controlled Autolab potentiostat PGSTAT100 (Metrohm), with Ag/AgCl as a reference electrode (RE) and Pt mesh as a counter electrode (CE). All potentials in this work are reported with respect to Ag/AgCl electrode (0.22 V *vs.* standard hydrogen electrode, SHE). The area of the working electrode (WE) exposed to the electrolyte was 0.07 cm$^2$. Cu foil was used as electrical contact around the circumference of the WE. For each experiment a fresh TiN/Si coupon pre-treated with 2% vol. HF (Alfa Aesar) for 2 min was used. Pt was electrodeposited on TiN coupons using galvanostatic deposition, at room temperature (21 °C) and without agitation. After Pt deposition, samples were immediately removed from the solution, rinsed with de-ionized water and dried in nitrogen flow. Characterization of PVD TiN, PVD Pt, and ECD Pt films was performed using SEM (Philips-XL30 ESEM), AFM (Nanoscope IVa Dimension 3100; Tapping mode), and X-ray diffraction (Bragg–Brentano setup, CuKα source, PANalytical). A four-point probe (HP4156c) was used to determine the sheet resistance of continuous Pt films.

Larger samples were plated using custom made 2-electrode set-up, with parallel-plate Teflon holders. One of the holders accommodated WE samples up to 10 × 10 cm in size, and the other one Ti plate as a counter electrode. Electrical contact was made along the circumference of the samples using Cu foil and self-adhesive Cu tape, which were then isolated from the electrolyte using Teflon self-adhesive tape. The 2-electrode setup was dipped vertically into a glass beaker and connected to a computer controlled Autolab potentiostat PGSTAT100. The electrolyte was agitated using magnetic stirrers.

First Pt interconnects were fabricated on 2 inch (diameter) TiN/polyimide/glass substrates.

VM-652 (HD Microsystems) was used as an adhesion promoter between the polyimide PI-2611 (HD Microsystems) and glass. HD-4110 (HD Microsystems) and 70 nm thick PVD TiN completed the stack on TiN/polyimide/glass wafers. S1828 positive photoresist (Rohm and Haas Electronic Materials Europe, Ltd.) was coated on TiN and used to define patterns for Pt plating. Photolithographic definition of resist pattern was done using a mask designed with CleWin 3.1 software. The pattern consisted of interconnects with different pitches and different line widths (20, 50, and 100 μm) and different pitches (1:1, 1:2, and 1:5). S351 'developer' (Rohm and Haas Electronic Materials Europe, Ltd.) was used to develop the pattern after exposure. Pattern fidelity, Pt line uniformity and defectivity were examined using optical microscopy and SEM after resist-strip, and then again after TiN etching. Dektak surface profiler and four-point probe measurements were used to estimate the thickness and resistivity of Pt lines, respectively.

## 3. Results and discussion

Galavanostatic plating experiments were performed at current densities ranging from −0.1 to −10 mA cm$^{-2}$. Fig. 1 shows selected potential-log (time) responses during early stages of Pt deposition from dihydrogendinitrosulfatoplatinate solution. Qualitatively, these responses could be described using theory of galvanostatic nucleation and growth detailed in references [11,12]. Time required for the potential to reach the peak value, decreased with increase in deposition current density. The peak potential attained the most negative value for the highest (absolute value of) current density. Please note that in this paper negative current density designate cathodic currents. Initial potential drop to more negative values could be ascribed to charging of the electric double layer and formation of subcritical islands. Critical overpotential is reached at some point in time before the peak, and supercritical is-
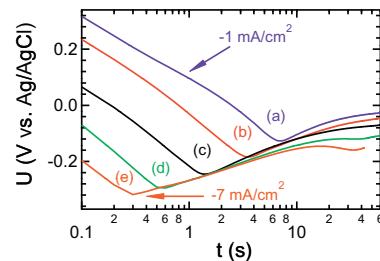


Fig. 1. Potential-time transients in a semi-log scale for galvanostatic deposition from 36 mM dihydrogendinitrosulfatoplatinate(II) solution at (a) −1, (b) −2, (c) −3, (d) −5, and (e) −7 mA cm$^{-2}$.

lands are formed. Their population is continuously increasing through the peak in potential, and up to the point in time when potential increases again to the critical value. Beyond this point, no new supercritical islands are created, while potential is steadily increasing and at long times reaches a steady value. Critical overpotential can be determined experimentally through implementation or rather demanding methods [11,12], which were deemed beyond the scope of this study. We limited ourselves to observation of saturation (final) island density, in order to determine the optimal current density for deposition of Pt interconnects. On one hand, we wanted to be imaging surface and islands after no new islands were formed, but on the other hand we also wanted to allow easer counting by stopping deposition before islands started coalescing into a continuous film. From time-evolution of island density (not shown) we have determined that the ideal deposition time was defined by the consumption of −0.03 C cm$^{-2}$ of charge density. Top-down *ex situ* SEM images (Fig. 2a,c) show Pt islands deposited at −1, −3, and −7 mA cm$^{-2}$ on the surface of the TiN electrode, with transients stopped once the charge of −0.03 C cm$^{-2}$ was reached. The saturation island density ($N_0$) was the highest at $4 \times 10^{10}$ cm$^{-2}$ for deposition at −3 mA cm$^{-2}$ (Fig. 2d). And while this result contradicts what we would expect to observe based on the form of our potential-time transients and the theory o galvanostatic nucleation and growth, one has to keep in mind that the theory does not account for parasitic currents which may be a significant fraction of total current for deposition in the range −4 to −10 mA cm$^{-2}$. This could be one of the reasons for the drop in island density at higher current densities. We have also monitored potential-time responses during late stages of deposition, i.e. long after islands have coalesced into a continuous and growing film. Two transients displaying typical features of Pt film deposition on PVD TiN are shown in Fig. 3a. Both experiments were performed using the same electrolyte and the same current density of −3 mA cm$^{-2}$. The substrates were PVD TiN layers of similar chemical composition, but different thickness and roughness. The solid curve is the response obtained during plating on 30 nm thick TiN with roughness parameters RMS = 0.9 nm and Ra = 0.7 nm, while dotted curve corresponds to plating on TiN substrate 70 nm thick and having RMS = 2.6 nm and Ra = 2.1 nm. RMS and Ra were determined from 1 × 1 μm AFM images. To get a better idea of the difference in roughness between the two substrates, single AFM line scans were plotted in Fig. 3b. We emphasize this because, like many other researchers [6 and reference therein], we have tried to determine the key parameter and establish processing steps to improve adhesion between TiN and Pt layers. In agreement with previous findings [6], the increase in roughness of the TiN substrate lead to improved adhesion with electrodeposited Pt, and thicker films could be deposited on it. Above mentioned 70 nm thick PVD TiN was our 'champion' substrate and was used as a conductive layer for Pt plating on polyimide. The maximum Pt film thickness obtained on this TiN was about 800 nm. On the other hand, use of smoother