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journal homepage: [www.elsevier.com/locate/mejo](http://www.elsevier.com/locate/mejo)Memristor based  $N$ -bits redundant binary adderA.A. El-Slehdar<sup>a</sup>, A.H. Fouad<sup>a</sup>, A.G. Radwan<sup>a,b,\*</sup><sup>a</sup> NISC Research Center, Nile University, Cairo, Egypt<sup>b</sup> Engineering Mathematics and Physics Dept., Faculty of Engineering, Cairo University, Cairo, Egypt

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## ABSTRACT

This paper introduces a memristor based  $N$ -bits redundant binary adder architecture for canonic signed digit code CSDC as a step towards memristor based multilevel ALU. New possible solutions for multi-level logic designs can be established by utilizing the memristor dynamics as a basis in the circuit realization. The proposed memristor-based redundant binary adder circuit tries to achieve the theoretical advantages of the redundant binary system, and to eliminate the carry (borrow) propagation using signed digit representation. The advantage of carry elimination in the addition process is that it makes the speed independent of the operands length which speeds up all arithmetic operations. One memristor is sufficient for both the addition process and for storing the final result as a memory cell. The adder operation has been validated via different cases for 1-bit and 3-bits addition using HP memristor model and PSPICE simulation results.

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## 1. Introduction

Due to future physical limitation on transistor scaling in the semiconductor industry [1], scientists and engineers have started working on new nano-elements that can improve the performance of the electronic circuits. One of these promising elements is the memristor which was postulated by Chua [2] and physically realized by HP-lab in 2008 [3] as the missing fourth fundamental element. The memristor stands as a new candidate, holding great promise for changing hardware computation towards faster and more power efficient designs due to its nanoscale size and its analog memory capability. One of the memristor characteristics is that its  $I-V$  plot has a pinched-hysteresis loop, which means its resistance has a continuous range [2]. The memristor is an element whose state is stored in its memristance, which changes depending on the charge or flux passing through it [4–6]. Recently, many memristor-based logic circuits were presented such as: analog addition and subtraction circuits [7], digital circuits using implication logic [8,9], binary logic circuits [10], and half adders based on ternary and redundant systems [11,12]. Moreover, the memristor has been involved in many applications such as oscillators [13,14], modified neuron model [15,16] and graph theory [17].

Multilevel arithmetic operations have many advantages over the binary representation in terms of speed and memory usage [18,19].

Generally, the investigation of the arithmetic operations in other radixes (other than binary) or when allowing additional values becomes an interesting topic, where each digit in any number system is defined by a set of values. For example; each digit in the decimal system uses the set  $\{0, 1, 2, \dots, 9\}$ , the conventional position weighted binary number system uses the set  $\{0, 1\}$ , and the binary signed digit (redundant number system) uses the set  $\{\bar{1}, 0, 1\}$  (where ' $\bar{1}$ ' is equivalent to ' $-1$ ') [16]. A number ' $x$ ' can be represented using signed digit code as follows:

$$\sum_{i=0}^{W_d-1} x_i w_i, \quad (1)$$

where ' $W_d$ ' is the operand length and ' $w_i$ ' is the weight of each digit, depending only on the position of the digit ' $x_i$ ', where  $x_i = \bar{1}, 0$  or  $1$ . To eliminate the carry (borrow) from rippling, unconventional redundant numbering systems are often used in certain application-specific arithmetic units [19]. One of the famous unconventional redundant representations is the Canonic Signed Digit Code (CSDC) representation, which can be written as follows:

$$\sum_{i=0}^{W_d-1} x_i 2^i. \quad (2)$$

CSDC is a special case of Signed Digit Code (SDC), where any two consecutive digits must include at least a ' $0$ ', so converting from SDC to CSDC can be done by transforming every  $[011\dots 1]$  and  $[0\bar{1}\bar{1}\dots \bar{1}]$  to a series of zeroes between ' $1$ ' and ' $-1$ '  $[100\dots \bar{1}]$  and  $[\bar{1}00\dots 1]$ , respectively. Table 1 shows the result of adding two CSDC digits ' $x$ ' and ' $y$ ' together, where the outputs ' $s$ ' and ' $c$ ' are

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the sum and the carry, respectively. Moreover, Eq. (3) shows how the carry can be eliminated in case of adding two numbers 'X' and 'Y' in CSDC form, with a length of 'n' digits and represented as { $x_{n-1} x_{n-2} \dots x_1 x_0$ } and { $y_{n-1} y_{n-2} \dots y_1 y_0$ }, respectively.

$$\begin{array}{r} x_{n-1} \ x_{n-2} \ \dots \ x_1 \ x_0 \\ y_{n-1} \ y_{n-2} \ \dots \ y_1 \ y_0 \\ \hline s_{n-1} \ s_{n-2} \ \dots \ s_1 \ s_0 \\ \hline c_{n-1} \ c_{n-2} \ c_{n-3} \ \dots \ c_0 \ \_ \\ z_n \ z_{n-1} \ z_{n-2} \ \dots \ z_1 \ z_0 \end{array}, \tag{3}$$

where ' $s_{n-1}$ ', and ' $c_{n-1}$ ' are the sum and the carry result of adding the digits ' $x_{n-1}$ ' and ' $y_{n-1}$ ' following the truth Table 1, and ' $Z$ ' is the final result after adding the carry ' $C$ ' to the sum ' $S$ '. So, in order to have a propagating carry, both ' $x_1$ ' and ' $y_1$ ' must be equal to '1' and at least one of ' $x_2$ ' and ' $y_2$ ' should be equal to '1', which violates the CSDC property. Therefore, the CSDC addition can be always free of the carry propagation by generating the sum value and the carry value in parallel, then adding the carry to the sum, which can also be done in parallel. Let us assume the adding of ( $X = 35$ ) and ( $Y = -11$ ) as in Eq. (4); the result equals '24' as expected in two steps where each two bits are being added by a single full adder unit.

$$\begin{array}{r} 10010\bar{1} \\ 0\bar{1}0101 \\ \hline 1\bar{1}0000 \\ 001000 \\ \hline 01\bar{1}1000 \end{array} \tag{4}$$

By speeding up the arithmetic addition without the carry propagation, the multiplication process could be improved due to the reduction in the number of addition and subtraction cycles. Recently, the concept of canonic signed digit has been used in

**Table 1**  
Truth table of the redundant full adder.

x	y	Decimal value	s	c
0	0	0	0	0
0	1	1	1	0
0	-1	-1	-1	0
1	0	1	1	0
1	1	2	0	1
1	-1	0	0	0
-1	0	-1	-1	0
-1	1	0	0	0
-1	-1	-2	0	-1

many applications like digital filters [20,21] and high speed multipliers [22].

The objective of this paper is to provide a general architecture for building an N-bit redundant binary full adder. Thus, two different problems should be addressed: the first one is having an element that is efficient enough to store more than two states (on and off states) without adding extra hardware, and the second one is to build an adder circuit whose speed is independent of the operands length (parallelizing the addition process), which is impossible using the conventional number systems.

The first challenge can be solved by using a memristor and quantizing its memristance range into levels, each level has a certain memristance sub-range. The second challenge can be solved by designing a memristor-based redundant binary adder, using the memristor's capability to process and store three states. Since its speed performance is independent of the operands' length, a cascaded N-stages adder can be achieved without the need of extra hardware. Another advantage of this adder is that the output will be automatically stored until the next output is generated. Therefore, the proposed design is equivalent to a full adder followed by a memory unit.

**Table 2**  
Truth table of the redundant full adder.

X	Y	Z	Sum	Carry	Decimal value
-1	-1	-1	-1	-1	-3
-1	-1	-1	0	-1	-2
-1	0	1	0	0	-1
-1	0	-1	-1	0	-1
-1	0	0	0	0	0
0	1	0	1	0	1
0	0	1	1	0	1
0	0	0	0	1	2
1	1	0	0	1	2
1	1	1	1	1	3

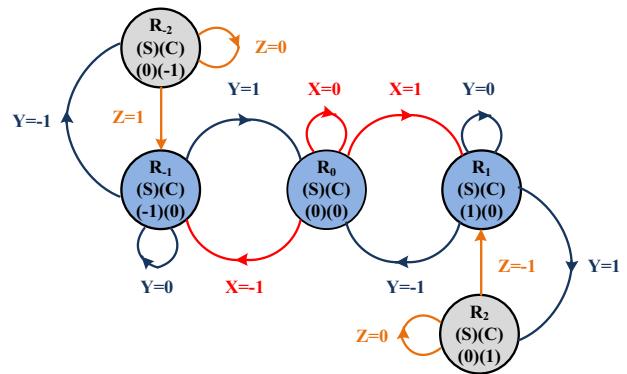


Fig. 2. Full adder graph representation.

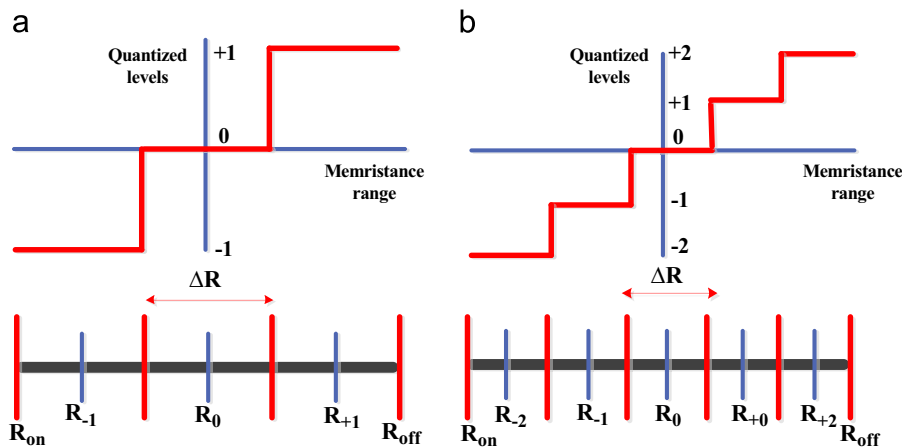


Fig. 1. Quantizing memristance (a) three levels quantization, and (b) five levels quantization.

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