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# Quantifying the effect of local interconnects on on-chip power distribution

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ABSTRACT

Existing methods to analyze and optimize on-chip power distribution networks typically focus only on global power network modeled as a two-dimensional mesh. In practice, current is supplied to switching transistors through a local power network at the lower metal layers. The local power network is connected to a global network through a stack of vias. The effect of these vias and the resistance of the local power network are typically ignored when optimizing a power network and placing decoupling capacitors. By modeling the power distribution network as a three-dimensional mesh, the error due to ignoring via and local interconnect resistances is quantified. It is demonstrated that ignoring the local power network and vias can both underestimate (by up to 45%) or overestimate (by up to 50%) the effective resistance of a power distribution network. The error depends upon multiple parameters such as the width of local and global power lines and via resistance. A design space is also generated to indicate the valid width of local and global power lines where the target resistance is satisfied. It is shown that a wider global network can be used to obtain a narrower local network, providing additional flexibility in the physical design process since routability is an important concern at lower metal layers. At high via resistances, however, this approach causes significant increase in the width of a global power network, indicating the growing significance of local power network and vias.



## 1. Introduction

Robust and reliable power delivery is a critical challenge in modern, high performance integrated circuits (ICs) due to lower operating voltages, relatively higher switching currents, and faster transition times [1,2]. Parasitic resistance and inductance within a power distribution network cause both static and dynamic voltage fluctuations, typically characterized as $I(t)R$ drop and $L\,di/dt$ bounce. These fluctuations degrade *power integrity* and have three deleterious effects on circuit operation: (1) delay uncertainty since transistor delay is a strong function of the power supply voltage, (2) degradation in gate insulator reliability due to possible overshoots, and (3) in extreme cases, logical failure.

In the frequency domain, a power distribution network is analyzed to satisfy a *target impedance* within the frequency range of interest [3,4]. The target impedance is determined from the nominal supply voltage, tolerable noise, and average load current. According to ITRS 2011, by 2026, the nominal supply voltage is expected to scale down to 0.57, 0.43, and 0.54 V, respectively, for high performance, low operating power, and low standby power ICs [5]. Furthermore, the average current drawn by the load circuit increases due to greater functionality and higher static leakage current [5]. These two trends exacerbate the process of power delivery by significantly reducing the target impedance. Thus, modern power distribution networks consume a significant portion of the on-chip metal resources [1].

Efficient and sufficiently accurate analysis of power distribution networks plays an important role not only in quantifying power supply noise, but also optimizing the physical characteristics of a power network and placing decoupling capacitors [6,7]. Despite an increasing number of studies that implies the growing importance of local interconnects, there is still a significant amount of recent work that ignores these effects in analyzing and optimizing a power network [2,8–13]. These works utilize a two-dimensional model of a global power distribution network structured as a grid, as illustrated in Fig. 1. In [10], authors investigate the effect of vias only within the global power network. Local power grid and the vias between the local and global grids are not considered.

The commonly used model as shown in Fig. 1 ignores the *local* power distribution network at the lower metal layers (such as M1 and M2) and the *stack of vias* used to connect the global and local power networks. In [14], Shelar and Patyra have investi gated the impact of local *data* interconnects on timing and power

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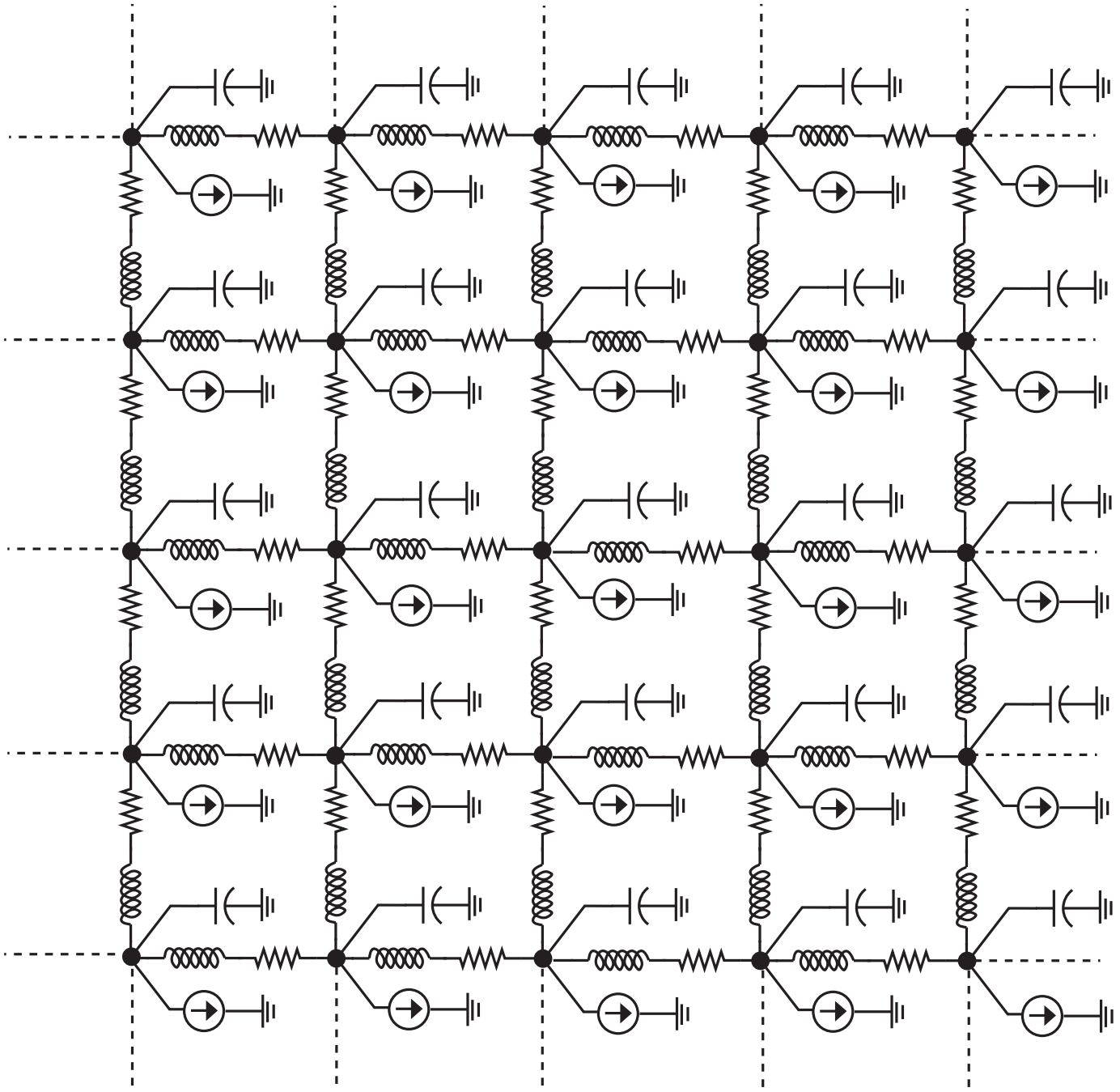

**Fig. 1.** Model of an interdigitated, global power distribution network that ignores the local power network and stack of vias connecting global and local power networks.

characteristics of a high performance microprocessor, demonstrating the non-negligible influence of these interconnects. The effect of local *power* interconnects and stack of vias on power integrity, and the dependence of this effect on metal widths, however, have not received much attention. In [15,16], local power network has been considered during power supply noise estimation. In [17], vias have also been included to analyze power supply noise. The primary research emphasis, however, has been on reducing the computational complexity and memory requirements of the analysis process. Error due to ignoring local power network and vias has not been investigated. This issue has become more significant since the via resistances increase with each technology node [5].

The primary contributions of this work are as follows: (1) the error in effective resistance due to ignoring local power network and vias is quantified, (2) the dependence of this error on metal width and via resistance is evaluated, (3) under constant physical area and metal coverage for the global power network, a design space is developed to determine the range of metal width where the target resistance is satisfied. The effect of via resistance on the design space is also investigated.

The rest of this paper is organized as follows. A power distribution network model considering both global and local power networks is described in Section 2. Analysis framework, methods used to achieve efficient and sufficiently accurate analysis of the model, and results quantifying the significance of local power network and vias are provided in Section 3. The paper is concluded in Section 4 and possible future work is discussed in Section 5.