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A 2.45-GHz W-level output power CMOS power amplifier with adaptive bias and integrated diode linearizer

Zhi-xiong Ren, Ke-feng Zhang*, Lan-qi Liu, Xiao-fei Chen, Dong-sheng Liu, Zheng-lin Liu, Xuecheng Zou

School of Optical and Electronic Information, Huazhong University of Science and Technology, 430074 Wuhan, PR China

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ABSTRACT

A high-linearity CMOS power amplifier (PA) operating at 2.45 GHz for WLAN applications with adaptive bias and an integrated diode linearizer is presented. The PA adopts adaptive bias scheme to adjust the gate bias voltage of power transistors by tracking the output power of the first diver amplifier for efficiency enhancement. Diode-connected MOS transistor is used to compensate the nonlinearity of input capacitance (C_{gs}) of power transistors for linearity improvement. The simulation results demonstrate a gain of 33.2 dB, a maximum output power of 30.7 dB m with 29% of peak power added efficiency (PAE) and −30 dBc third-order intermodulation (IMD3) product at 26.4 dB m output power, reaching to excellent tradeoffs between efficiency and linearity.

1. Introduction

Power amplifier (PA), as a bottleneck to realize fully integrated CMOS transceiver, is still largely fabricated using GaAs, SiGe and other III–V compound technologies, though CMOS PA had been successfully proposed [1]. Because of the inherent disadvantages of CMOS technology, such as low breakdown voltage, low-resistivity substrate, etc., CMOS PAs are mainly limited to switched operating mode [2–4], which can settle with moderate linearity due to the low peak to average power ratio (PAPR) of the signal. As the complexity of signal modulation increases with the data transmission rate, much more attention had been paid on the linear CMOS PAs used in WCDMA, WLAN, and WiMax [5–8], etc. Therefore, in order to meet the strict requirements of these communication protocols, the methods on improving output power, linearity, and efficiency had been incorporated in the design of CMOS PAs.

On-chip transformer-based power combiner is widely adopted for higher output power, to solve the problems of low breakdown voltage of MOS transistor, which is more serious due to the lower supply voltage with the scaling of CMOS technology. DAT utilizing "slab" inductors presented in [2–4] has also proven on-chip transformer-based power combiner reliable and effective to realize W-level output power. Parallel-series combining transformer (PSCT), series combining transformer (SCT) and parallel combining transformer (PCT) with complicated interwoven windings have been analyzed in detail and successfully applied to linear and switched PAs [6,7,9]. Power combiner is also an effective method to improve average efficiency at power back-off by switching the combined sub-PAs.

As to linear CMOS PAs design, there are many techniques to resolve the tradeoffs between linearity and efficiency. Compared with dynamic power supply requiring a complicated DC–DC converter, adaptive or dynamic bias scheme [10,11] is a relatively simple way to improve the PAE of PA in frequently used low power region, particularly important for 2.4 GHz WLAN application adopting OFDM modulation [8]. The linearization techniques can be categorized as technology-level, circuit-level and system-level. Technology-level linearization techniques had been widely adopted in CMOS PAs to linearize the non-linearity of MOS, such as C_{gs} and C_{jd} [12]. Circuit-level techniques including MOS compensation [13], harmonic termination [14], and diode linearizer [15–17] were also widely used in CMOS PAs to cancel the harmonics generated by C_{gs} and g_{m3}. Diode linearizer was utilized in HBT MMIC PA for the first-time [15,16], and its effectiveness had also been proven in CMOS PA design [17]. System-level linearization techniques, such as digital pre-distortion (DPD) [18], Doherty PA [19], Cartesian feedback [20], etc., are effective to enhance the linearity of PA, but they take considerable chip area and dc power consumption. Moreover, the transmitted noise resulting in the higher sensitivity requirement of receiver puts stringent linearity requirement of PA, which will compromise the overall transmitter

* Corresponding author. Tel.: +86 13986226880.
E-mail address: zhangkefeng@hust.edu.cn (K.-f. Zhang).

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power efficiency and complicate output power control. Therefore, the noise analysis of each block in this PA is addressed.

In this paper, we combine adaptive bias with diode linearizer (ABDL) to improve the efficiency in the back-off mode and linearity at the high output power level simultaneously without sacrificing chip area and power consumption. The fully integrated CMOS PA operating at 2.45 GHz consists of input match balun, one driver amplifier, three power amplifiers, on-chip parallel-combining transformer (PCT) and ABDLs. According to the simulation results, the proposed ABDL increases the average efficiency of PA at power back-off region and improves IMD3 from −30 dBc@P_{out}=14.5 dB m to −30 dBc@P_{out}=25.5 dB m, compared with constant 560 mV bias voltage. The proposed linear CMOS PA achieves a gain of 33.2 dB, a maximum output power of 30.7 dB m with 29% of peak PAE.

This paper is organized as follows. In Section 2, the proposed power amplifier including the all design building blocks, such as input match, output power combiner, adaptive bias and diode linearizer will be described. In Section 3, the noise of input balun, power combiner, driver and power stage is analyzed and simulated. In Section 4, the post-layout simulation results of the proposed CMOS PA will be presented, discussed in details and finally compared to those of the recent works. Section 5 concludes this work.

2. Circuit design

2.1. Proposed power amplifier

The schematic diagram of the designed CMOS PA is shown in Fig. 1. For watt-level output power requirement of WLAN applications, three parallel power amplifiers are incorporated through on-chip PCT [9]. The PCT performs not only the power combining, but also the impedance down-transformation. There are resonant capacitors at the input and output port of the PCT for optimal performance at the specified operating frequency, and no additional output matching networks are required. The power amplifier is composed of inter-stage coupling capacitors, diode linearizers and self-biased cascode amplifiers consisting of the thin-oxide 0.18 μm common-source (CS) and the thick-oxide 0.35 μm common-gate (CG) for higher voltage stress. The driver amplifier also adopts self-biased cascode amplifiers with the 0.18 μm CS and CG for 1.8 V VDD_DA supply voltage. Self-biasing had been proven an effective technique to relax the restriction due to hot carrier degradation in power amplifiers [21]. On-chip transformer as input balun with input and output resonant capacitors is used to realize the 50 Ω input match and single-to-differential transformation. Adaptive bias circuit tracking the output AC signal of the driver amplifier generates DC bias voltage for the power amplifier. The equivalent circuit model of bonding wire is also included in the fully integrated CMOS PA design.

2.2. Inductive components

The performance of PA is greatly affected by the quality of on-chip passive inductive components, especially in CMOS technology. The inductive components shown in Fig. 2 used in the PA consists of the choke inductor in driver amplifier, input balun and output PCT. All windings of these inductive components are fabricated using top ultra-thick metal with 4.6 μm thickness. The choke inductor resonant with the inter-stage capacitor at 2.45 GHz is a high-Q (quality) differential circular inductor with center-tap for 1.8 V power supply. The 3-turn differential inductor with the following geometrical parameters: width=15 μm, spacing=3 μm and inner diameter=80 μm. For higher current density, the center-tap metals are composed of three-layer parallel metals. The single-ended effective inductance, resistance and Q of the inductor with floating poly-silicon pattern ground shield (PGS) are shown in Fig. 3.

The symmetrical input balun with 1:3 turn ratio transforms the high input resistance to 50 Ω and the primary and secondary windings are 10 μm width, 300 μm outer dimension (OD), and 3 μm gap between them. The PCT is composed of three primary windings and one secondary winding with 1:2 turn ratios. The windings are 30 μm width and the spacing between them is 4 μm. The EM simulated insertion losses of input balun and PCT are 1.32 dB (73.8%) and 1.31 dB (73.83%) at 2.45 GHz, respectively, as shown in Fig. 4. The expressions to calculate the efficiency in terms of the two-port S-parameters are given as follows:

$$\text{Efficiency} = \left|\frac{S_{21}}{S_{12}}\right|\left(k-\sqrt{k^2-1}\right) \quad (1)$$

where

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad (2)$$

The above on-chip inductive components are designed and simulated using Agilent's Momentum 2.5D electromagnetic (EM) simulator.

2.3. Adaptive bias

The proposed adaptive bias circuit consists of power detector, which uses the nonlinearity of i_{ds} of NMOS transistor (M1, M2), and PMOS bias adjusting circuit (M5) as shown in Fig. 5. The NMOS M1 and M2 in Fig. 5 detect the power of RF input signal, changing into DC voltage proportional to RF input power, based on

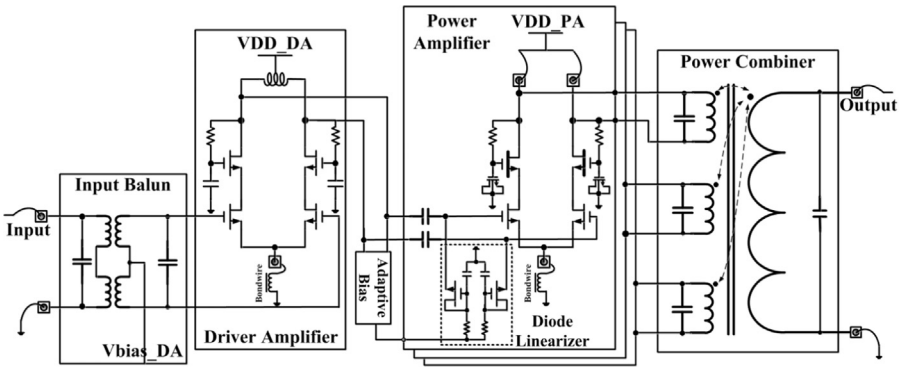

Fig. 1. Schematic diagram of the PA.