Microelectronics Journal 46 (2015) 343–350

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Modeling single event crosstalk speedup in nanometer technologies

Selahattin Sayil *, Li Yuan

Department of Electrical Engineering, Lamar University, P.O. 10029, Beaumont, TX 77710, USA

ARTICLE INFO

Article history:
Received 14 March 2014
Received in revised form
28 September 2014
Accepted 5 February 2015
Available online 13 March 2015

Keywords:
Single event crosstalk
Signal speedup
Best-case delay modeling

ABSTRACT

With advances in CMOS technology, circuits become increasingly more sensitive to transient pulses caused by single event (SE) particles. In addition, coupling effects among interconnects can cause SE transients to spread electronically unrelated circuit paths which may increase the SE Susceptibility of CMOS circuits. The coupling effects among interconnects need to be considered in single event modeling and analysis of CMOS logic gates due to technology scaling effects that increase both SE vulnerability and crosstalk effects. This work reports on the signal speedup effects caused by SE crosstalk and then proposes a best-case delay estimation methodology for use in design automation tools for the first time to our knowledge. The SE coupling speedup expressions derived show very good results in comparison to HSPICE results. Results show an average error of about 8.42% for best-case delay while allowing for very fast analysis in comparison to HSPICE.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

Terrestrial soft errors in memory have been a very well-known problem [1]. However, due to increasing clock frequencies and shrinking feature sizes soft errors are now affecting CMOS logic. It was predicted that below 65 nm technologies, the majority of the observed radiation induced soft failures will be due to transients that will occur in combinational logic (CL) circuits [2].

Researchers mostly considered single event transients (SETs) as the main cause for combinational logic (CL) related radiation-induced soft errors. However, for high-reliability, mission-critical applications such as avionics [3], medical systems [4], etc., additional sources such as single event (SE) coupling effects must also be included in analysis in addition to SETs.

An SET generated on a circuit node is no longer limited to the logic path existing between the hit node and a latch due to increasing coupling effects. The coupling effects can cause SETs to contaminate electronically unrelated circuit paths which can in turn increase the “SE Susceptibility” of CMOS circuits to SETs [5–7].

Due to decreased spacing and increased thickness to width ratio of interconnects, increasing coupling effects occur as technologies advance. The interaction caused by parasitic coupling between wires, which is generally known as crosstalk, may cause undesired effects such as noise glitches, signal delays or even delay reductions [8–10]. Among these effects, the crosstalk glitch effects occur when there is a voltage transition in one or more of several coupled lines. In this case, other non-switching (victim) wires suffer a voltage perturbation or a glitch. If the crosstalk glitch generated on the victim line is large and propagates into a storage element during its latching window, incorrect data storage will occur.

It is no longer just the normal signal switching events on aggressor (affecting) lines that are responsible for such crosstalk noise and speedup effects [5–7]. As technology scaling continues, the charge deposited due to an SE particle on aggressor line may also create increasing cross-coupling noise effects, and in some cases the effects can be larger than a normal switching induced crosstalk.

Balasubramanian et al. have shown that SETs can induce crosstalk noise effects on neighboring lines that can create logic level state changes for interconnects as small as 100 μm on technologies 90 nm and lower [5]. In [11], the SE induced crosstalk noise effect has been experimentally measured in a 90 nm process and this proved the existence of the problem.

Later work in [12] also studied the effect of interconnect coupling and Miller effects on SET propagation. Finally, the work in [7] compared SET and SE crosstalk noise (SECN) effects in detail and studied SE crosstalk error rate contribution using some benchmark circuits. Simulation results showed increasing circuit sensitivity to radiation when SE coupling effects included.

In addition to a crosstalk glitch, an SET generated on an aggressor wire (due to particle hits on driver transistors) may also cause delay changes on neighboring interconnect via cross-coupling effects if these lines are in switching. These delay changes may later violate setup or hold time requirements of logic storage circuits connected to these receivers.

In the example shown in Fig. 1, an SE particle hit at the drain of OFF PMOS transistor of the inverter driver causes the output to go towards logic 1 (or V_{DD}) for some pulse duration. The SET created, in turn, spreads into the victim line via coupling capacitance and

* Corresponding author. Tel.: +1 409 880 8756; fax: +1 409 880 8121.
E-mail address: sayil@lamar.edu (S. Sayil).

http://dx.doi.org/10.1016/j.mejo.2015.02.002
0026-2692/© 2015 Elsevier Ltd. All rights reserved.

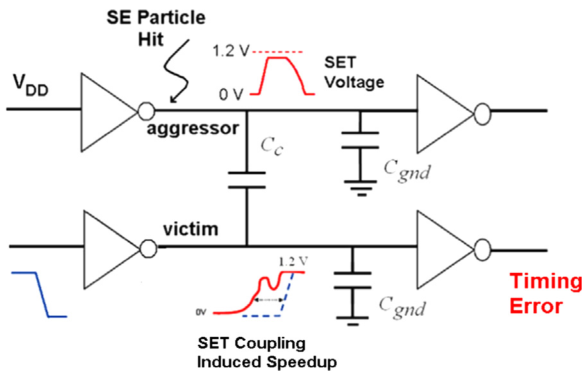

Fig. 1. SE crosstalk speedup (Lumped model is for demonstration only).

causes a speedup effect on the rising victim line waveform. As a result, victim line signal switches sooner than it would. This effect can be named as SE crosstalk speedup or SECS. The decrease in interconnect delay due to SET coupling can affect circuit performance as the speedup effects may later violate hold time requirements of logic storage circuits connected to these receivers [8].

Similarly, for a falling victim waveform, the positive SET voltage on aggressor line can cause increased signal delays on victim line [7,13] which can later translate into setup time violations of storage elements.

This work focuses on SE coupling induced speedup effects for the first time to our knowledge. It will be later shown that the SE transients can induce more speedup effects than normal switching signals would after a certain deposited charge. The effect of SECS also increases as device sizes further scale down. Hence, consideration of SE induced coupling speedup becomes very important in timing analysis.

Traditional SPICE simulators can be used to estimate crosstalk noise and delay effects in signal lines. While results are accurate, due to density of interconnect lines, these simulations are time inefficient [8–10]. A rapid and accurate crosstalk noise and speedup estimation alternative are needed to ensure acceptable signal integrity in a limited design cycle time so that one can quickly verify if a given wire routing solution will not lead to logic or timing failures caused by the coupled noise.

There have been some efforts in modeling SE crosstalk effects. The work in [14] proposed a fast SE crosstalk noise estimation method for use in design automation tools. Most recently, a similar modeling has been offered in [15] which used Taylor series expansions to further minimize runtime.

However, there has not been any work in modeling of SE coupling speedup effects to our knowledge. Circuit designers are usually interested in best-case delays; hence this work aims to calculate the best-case delay that can be induced on a victim line due to an SET on an aggressor line.

In our modeling, we ignore inductance effects, and assume capacitive effects are dominant for most on-chip wires [8–10].

This paper is organized as follows. Section II studies the SECS effects and compares to normal switching induced speedup. The effect of technology scaling has also been discussed in this section. Section III presents the proposed best-case delay estimation methodology. In this methodology, the SE crosstalk noise magnitude is needed for the best-case delay calculation. Hence, Section IV covers the SE crosstalk model in detail. This section first explains the 4-π interconnect model used, and then discusses on the SE current source modeling and driver representation. Modeling of passive aggressors and RC tree branches are also discussed in this section. Finally, the SE crosstalk voltage at victim-end is formulated in Section IV.

Section V summarizes the steps involved in the proposed best-case delay model. The model has been tested extensively using 1000 randomly generated circuits in 45 nm technology and results are verified using HSPICE. These results are shown in Section VI. Finally, we conclude in Section VII.

2. Analysis of single event coupling speedup

In this section, we first study SE crosstalk speedup effects and then compare to normal switching induced speedup to see if these effects are important.

When studying interconnect behavior, ideally a distributed model should be used to represent interconnect [8]. However, due to the complexity issues, the behavior is mostly approximated by sections of lumped circuit elements. In the simplest lumped RC model, the total resistance of the wire is lumped into one single resistance R and similarly the global capacitance of the wire is combined into a single capacitor C. However, this provides a very rough approximation of the actual transient behavior of interconnect.

The accuracy of the simple lumped RC model can be improved by dividing the total line capacitance into two equal parts, as shown in Fig. 2. This representation is named as the π-model representation [9].

More accurate representations of the distributed RC circuit can be obtained by using multiple-π segments (Fig. 3). The accuracy of this model increases with increasing number of segments N. Kawaguchi and Sakurai have reported that the error in simulating delay of the distributed RC line by using 5-π segment is less than 1% for almost all cases [16].

Nevertheless, researchers often use the 10-π model, to represent the distributed RC line in simulations. In our simulations, a 10-π model with distributed coupling capacitances is used for every 100 μm of wire to represent the RC distributed behavior (see Fig. 4).

In our simulations, two parallel interconnects that are on the intermediate layer are considered. For 90 nm technology, the wire dimensions taken were as follows [17]: the width (W), spacing (S) is 0.2 μm, and wire thickness T is 0.45 μm. For 65 nm technology, the dimensions were $W=S=0.14$ μm, and $T=0.35$ μm. Finally, for 45 nm technology, $W=S=0.1$ μm, and $T=0.24$ μm.

A wire length of 1000 μm is selected for the intermediate wire. It is assumed that aggressor and victim drivers and the loads at the end of the wires are minimum sized identical inverters.

In order to analyze the SE induced crosstalk speedup, a rising pulse waveform with a 100 ps rise time has been applied to victim driver while aggressor driver was kept at V_{DD} as shown in Fig. 4. Normally, aggressor driver output would be at "logic low" but it would be taken to "logic high" if there is a sufficient SE hit charge on output node of the driver.

An SE hit is simulated at the output of the aggressor driver using a double exponential current pulse in our analysis here. The hit charge was increased up to 150 fC in our simulation. At the end of the victim line, two inverters have been used to filter out the distortion on victim line and the signal delay is measured at V_{OV2}.

When comparing the SE crosstalk speedup to the normal aggressor switching induced speedup, the SE current source has been removed and then the aggressor driver is switched in same direction to the victim to simulate normal crosstalk speedup.

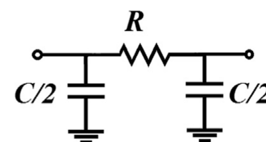

Fig. 2. π-model representation.

Download English Version:

https://daneshyari.com/en/article/541358

Download Persian Version:

https://daneshyari.com/article/541358

Daneshyari.com