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VLSI interconnect issues in definitive and stochastic environments

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ABSTRACT

A system designer needs to estimate the behavior of a system interconnection based on different patterns of switching which happen around an interconnect. Two different scenarios are supposed to estimate the effect of interconnect issues on system performance. *First*, based on a normalization technique for decreasing the number of a transfer function variables, a definitive environment for one interconnect is considered and an optimized look-up-table for the wire time delay is generated. Using some sampling methods, fast accessible look-up-tables are proposed for CAD tools in very simple and small one. A $4\times4\times4$ table for the wire delay is introduced which results in very fast estimation. The average and maximum error of this look-up-table is less than 1% and 7.7% respectively, compared to HSPICE results. *Second*, the statistical environment of a wire in a BUS configuration is studied for all possible different switching patterns happening for the wires. Estimating the BUS main problems, including power consumption, crosstalk, and propagation delay for a random environment, which a wire senses in wide BUS, is only possible with statistical parameters like mean and variance. All simulations are done considering both wire inductive and capacitive couplings in HSPICE. Also, the secondary effect of crosstalk on propagation delay and power consumption is considered. The simulation results show 3.81% of BUS input switching can lead to a wrong decision on its wire load due to the crosstalk induced voltages in 90 nm technology. The average induced crosstalk aware power consumption is 94 μW. Also, the average of maximum crosstalk on the load can be as high as 25% of the V_{dd}.

1. Introduction

High density state-of-the-art integrated circuits, ICs, are micro-electronic products. As the frequency and complexity of a chip increase, the number of its elements grows. Interconnects are the main components of digital integrated circuits. Increasing the number of elements results in more wiring density and complexity. Crosstalk noise causes power dissipation. If the crosstalk voltage amplitude exceeds the wire gate threshold voltage, a logic fault may occur and can transfer to the succeeding gate. Crosstalk analysis is addressed in Refs. [1–5]. Zhang in Ref. [5] has shown that Crosstalk noise can be as high as 37% of V_{dd}. Some researchers have investigated interconnects power consumption [6,7]. As reported in Ref. [8], up to 70% of on-chip capacitances are due to wiring interconnects. For a 130 nm microprocessor, more than 50% of the dynamic power consumption is due to interconnects, [9]. As the technology shrinks the power consumption of active devices reduces, and relatively interconnects power dissipation increases. Propagation delay variations may confine bit rate and maximum achievable frequency. The complexity of handling such vast number of wires and interconnects in digital systems are obvious. The statistical method is the only answer to this question. There are a lot of researches for statistic of the wire distribution in digital systems. Most of them are for introducing an accurate interconnects distribution function, *IDF*, like in Refs. [10,11]. Having the *IDF*, one can predict the wiring issues, such as power, delay, and the crosstalk in entire IC. Some works like Ref. [4] has fitted an expression of coupled lines for delay. The maximum error is less than 8% for 5 coupled lines for opposite and same switching direction for aggressor and victim lines. In a VLSI integrated circuit, an interconnect faces stochastic environments. Usually, the literature researches consider a single wire in a definitive and ideal surrounding. However, the statistical analysis requires handling with huge number of input and data. As we have different statistical process variations in technology, wire physical dimensions like width, spacing, length, and surface roughness have random distribution around their nominal values. The central limit theorem imposes that density function to be Gaussian with a nominal mean and variance. Agarwal in Ref. [12] has developed statistical model for delay and crosstalk with dimension variations. The comparison of Monte Carlo simulations in HSPICE and its approach shows good agreements within one percent error for the mean value. Some others like Ref. [13] have proposed a statistical *RLC* model considering process variations for impulse response of the

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wire by using Weibull distribution. Although their work has enough accuracy, for BUS configurations with different switching patterns and random environment it is hard to apply such methods. Considering all effects of interconnect parasitic results in very complicated expressions for desired parameters, while ignoring them leads to very poor estimation and underestimation of the effects. For example, in Refs. [14–17] the authors addressed the interconnect responses to step and ramp input and derived expression for time delay and crosstalk with capacitive load. In Ref. [18] propagation delay is studied for a limited range of VLSI interconnects. Ref. [19] suffers from the lack of accuracy such that it is not usable by CAD tools. On the other hand, Ref. [20] has an algorithmic structure that is suitable for CADs, however, it ignores the inductance effect which leads to less accurate estimations.

Based on time and distance domain various techniques of Laplace equation are used to investigate transient expressions, time delay, and crosstalk in single and coupled lines. However, no general solution has been offered up to now. For instance, a six-variable resistance per unit length, inductance per unit length, capacitance per unit length, R, L, C, Length of interconnect, the buffer output resistance, R_d and the load capacitance, C_l transfer function of a typical transmission line are appeared in Ref. [19]. Nevertheless, the need of CAD tools to an accessible data is not addressed by this universal function. Dealing with six variables is, no doubt, full of twists and turns.

In this study, we consider an ideal environment for one interconnect and address a novel methodology generating optimized look-up-tables which demonstrate the time delay of typical interconnects using normalization technique. In addition, the statistical environment of a wire in a BUS configuration will be studied for all possible different switching patterns. Estimating the BUS main problems including power consumption, crosstalk, and delay for random environment is possible just with the statistical variables like mean and standard deviation.

The paper is organized as follows. In Section 2, the normalization of interconnect transfer function is presented. Also the sampling methods are introduced for extraction of some simple and easy-use look-up-tables for delay estimation. In Section 3 we investigate the effect of stochastic switching on interconnect issues, including propagation delay, crosstalk and power consumption. Simulations for huge number of the switching patterns for an 11 bits BUS are done in this section. Finally paper ends with conclusions and references.

2. Normalization of transfer function

2.1. Basic model of transmission line

A classical interconnect configuration is shown in Fig. 1. The wire is represented by a distributed *RLC* transmission line, where l is the interconnect length, and R, L, and C are the resistance, inductance, and capacitance per unit length, respectively.

The input source as a line driver is serially connected to a driver resistance. The load of interconnect is modeled as a capacitor which is an accurate enough model for the input of most of CMOS gates. This equivalent circuit is a linear time-invariant (LTI) system. For LTI systems, the time-domain response can be solved by an inverse Laplace transform. Transfer function from the input to the far end of a line with some modification as in Ref. [19], can be written as follows:

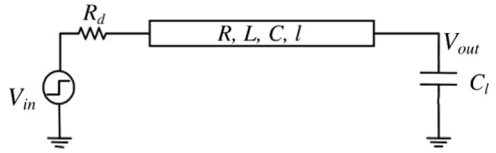

Fig. 1. Equivalent circuit model of a distributed *RLC* interconnect.

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=k_1(1+k_3)\frac{e^{-\theta\times l}}{1-k_2k_3e^{-2\theta\times l}} \tag{1}$$

where,

$$\theta=\sqrt{(R+sL)sC} \tag{2}$$

$$Z_c=\sqrt{(R+sL)/sC} \tag{3}$$

$$k_1=\frac{Z_c}{R_d+Z_c},\quad k_2=\frac{R_d-Z_c}{R_d+Z_c},\quad k_3=\frac{1-sC_lZ_c}{1+sC_lZ_c}. \tag{4}$$

where, Z_c is the characteristic impedance and θ is the propagation constant. Also R_d and C_l are the input driver impedance and load capacitance, respectively.

2.2. Normalization method

According to Ref. [26] normalizing the line (R, L, C, l, R_d and C_l) to a line with unity L, C, and l does not make any change in voltage transfer function (1). Thus, it would be more straightforward dealing with three variables instead of six while studying the line. The procedure of normalization is:

i) An *RLC* line with length l, can be replaced by a $(l\times R)(l\times L)(l\times C)$ line with unity length.
ii) Multiplication of all impedances of any linear circuit by a certain value does not change the voltage-voltage transfer function of the system; therefore, all impedances can be multiplied by the reciprocal *lossless* characteristic impedance of the line, Z_0.
iii) Finally, time–frequency duality implies that shrinking time by *time of flight*, *TF*, is the same as multiplying all frequencies by the same factor (*TF*).

Now, we have just three parameters for analyzing transfer function, r, R_d', C_l', the normalized resistance, the normalized buffer output resistance, and the normalized load capacitance, respectively. The r, R_d', C_l' represent all interconnect parasitic effects in addition to the driver and load values. As explained in i), ii), and iii) we have:

$$r=\frac{R\times l}{Z_0} \tag{5}$$

$$R_d'=\frac{R_d}{Z_0} \tag{6}$$

$$C_l'=\frac{C_l\times Z_0}{TF} \tag{7}$$

$$TF=l\sqrt{LC} \tag{8}$$

By continual wire width and thickness diminishing, the skin effect is showing itself for micrometer dimensions. For Copper at 1 GHz the skin effect is about 2.1 μm which is in the same order of the wire dimension. Therefore one should consider the skin effect carefully. As discussed earlier its normalization can be written as (9). The skin effect resistant variable is represented as R'. Due to its dependence to frequency, the normalized skin effect variable, r', depends on *TF* and Z_0 simultaneously.

$$r'=\frac{R'\times l}{\sqrt{TF}\times Z_0} \tag{9}$$