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Experimental characterization of coaxial through silicon vias for 3D integration

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Coaxial through silicon via (TSV) technology is gaining considerable interest as a 3D packaging solution due to its superior performance compared to the current existing TSV technology. By confining signal propagation within the coaxial TSV shield, signal attenuation from the lossy silicon substrate is eliminated, and unintentional signal coupling is avoided. In this paper, we propose and demonstrate a coaxial TSV 3D fabrication process. Next, the fabricated coaxial TSVs are characterized using *s*-parameters for high frequency analysis. The *s*-parameter data indicates the coaxial TSVs confine electromagnetic propagation by extracting the inductance and capacitance of the device. Lastly, we demonstrate the coaxial TSVs reduce signal attenuation and time delay by 35% and 25% respectively compared to the shield-less standard TSV technology. In addition, the coaxial interconnect significantly decreases electromagnetic coupling compared to traditional TSV architectures. The improved signal attenuation and high isolation of the coaxial TSV make it an excellent option for 3D packaging applications expanding into the millimeter wave regime.

1. Introduction

Three-dimensional integration (3Di) is an emerging packaging technology enabling vertical chip stacking. The performance, functionality, circuit density, and packaging efficiency are improved by stacking multiple chips [1]. Current 3Di efforts involve the integration of through silicon vias (TSVs) that interconnect multiple thin silicon die stacks. The current TSV structure consists of a $5 \times 50\ \mu m^2$ copper core with a surrounding dielectric oxide embedded within the silicon substrate. For radio frequency (RF) and high-speed applications, these TSVs are arranged in several orientations including the signal/ground (S/G) configuration [1–2]. In this orientation, the electromagnetic fields propagate between the signal and ground TSV as shown in Fig. 1. However, due to the poor dielectric properties of the low resistivity ($\rho = 10\ \Omega$-cm) silicon substrates used in complementary metal oxide semiconductor (CMOS) manufacturing, signal integrity is compromised. In addition, signal coupling and crosstalk can occur in adjacent vias or devices [3].

Recently several authors have proposed coaxial TSV technology to address the signal integrity concerns [5–8]. The coaxial TSV structure consists of a center metal core, inner dielectric oxide and surrounding metal ground shield as shown in Fig. 2. The coaxial TSV interconnect confines electromagnetic propagation within the structure by biasing both the core and shield. Specifically, the current in the shield is equal and opposite to the core current thus resulting in magnetic flux cancelation [9]. The coaxial TSV improves signal integrity by removing electromagnetic propagation from the lossy silicon substrate. In addition, the coaxial TSV prevents signal coupling to adjacent devices and circuitry.

In this work, we propose a coaxial TSV 3D interconnect that improves signal integrity over the frequencies of 20–65 GHz using 65 nm CMOS processing techniques. Section 2 describes our proposed device and fabrication within the confines of standard poly gate CMOS. Our test structure and results are discussed in Section 3. Lastly, we compare several key signal integrity metrics in Section 4 using our measured data for coaxial and S/G TSV structures.

2. Coaxial TSV design and fabrication

2.1. Coaxial TSV design

The coaxial TSV is intended to operate at frequencies greater than 20 GHz. The structure is designed to confine electromagnetic energy within its metal shield. For this reason, the current in the shield must be equal and opposite to the current in the core. At high frequencies, internal magnetic fields in the conductor force alternating current (AC) to be distributed about the perimeter of

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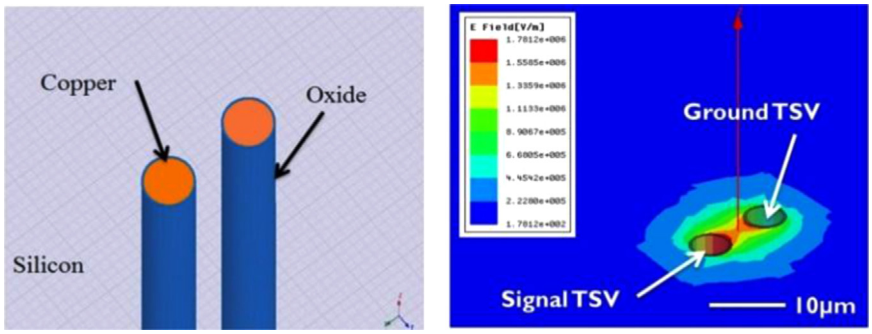

Fig. 1. The S/G TSV geometry and signal propagation created using Ansys' HFSS software [4].

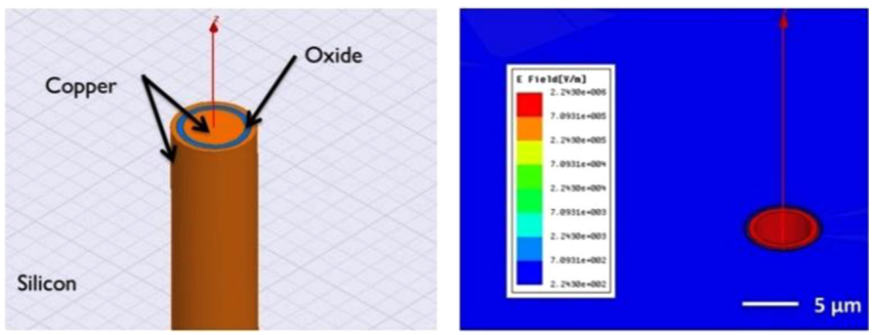

Fig. 2. The coaxial TSV geometry and signal propagation highlighting confined electromagnetic fields within the shield using HFSS [4].

the conductor. This phenomenon is known as the skin effect, which is dependent on the material conductivity and frequency of operation as shown in following equation [9]. We can create equal and opposite current flow by designing the shield of our coaxial TSV to be thicker than the conductor skin depth at frequencies greater than 20 GHz. The skin depth of copper versus frequency is shown in Fig. 3.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (1)$$

where the skin depth δ is dependent on the material resistivity ρ, frequency of operation f, and the permeability of the material μ.

Our coaxial TSV is designed to have a copper shield thickness of .5 μm. The core has a diameter of 5 μm that is consistent with the current traditional TSV structures. The inner dielectric separating the shield and core has a thickness of .5 μm due to process limitations. The traditional TSV, however, has a dielectric thickness of .1 μm by comparison [2]. For this reason, the total diameter of the coaxial TSV structure is 7 μm compared to the traditional TSV diameter of 5–5.5 μm. Lastly, both vias have a depth of 50 μm.

2.2. Coaxial TSV fabrication

The coaxial TSV fabrication process uses a standard via middle 3D method to create the structure [10–11]. We previously demonstrated the feasibility of coaxial 3D integration using a sputtering proves to form the copper shield [12]. This process includes using lithography and reactive ion etching (RIE) to construct the profile of the structure. Next, a .1 μm SiO_2 thin film is depositing into the via utilizing sub-atmosphere chemical vapor deposition (SACVD). The purpose of the first SiO_2 layer is to provide electrical isolation between the metal shield and silicon. We have since updated our shield process and incorporated a partial plating recipe to thicken the coaxial TSV shield to the .5 μm design specification. The process includes using physical vapor deposition (PVD) to deposit TaN as a diffusion barrier and Cu seed required for partial plating. Next, a thin film silicon nitride is deposited into the via using

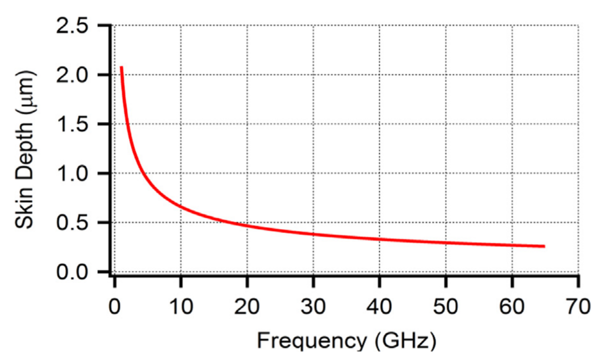

Fig. 3. The skin depth of copper versus frequency. At 20 GHz, the skin depth is approximately .5 μm.

chemical vapor deposition (CVD) to prevent copper diffusion into the inner dielectric SiO_2. The inner dielectric SiO_2 utilizes the SACVD technique to form .5 μm of oxide. Lastly, the core is filled using copper electroplating similar to traditional TSV formation. The excess surface material are then removed using chemical mechanical polishing (CMP).

At this step, the remaining wiring levels are formed on the front and backside of the wafer using both conventional copper damascene processing and 3D integration methods [13–15]. The wiring levels independently contact to the core and shield as required for electrical testing. A cross sectional image of the completed structure is shown in Fig. 4.

3. Coaxial TSV test structure and results

3.1. Coaxial TSV test structure

The RF testing capabilities on site include an Agilent N277A vector network analyzer (VNA) and Cascade Microtech Summitt 1200B semi-automatic probe station. The system is capable of making *s*-parameter measurements up to 65 GHz. Scattering