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A power efficient gain enhancing technique for current mirror operational transconductance amplifiers

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ABSTRACT

In this paper, a power efficient voltage gain enhancing technique is described. This technique is suitable for the amplifiers which use current starving method for gain enhancement (explained in the text). The proposed technique makes use of the current which conventionally goes to ground, through a parallel path. In this paper, the new technique is demonstrated for current mirror type of operational transconductance amplifier (OTA). Simulation results show that gain improves by a factor ~2, while consuming the same power as conventional OTA. The added advantage of this technique is that it does not affect the voltage swing while increasing the gain. Compared to the conventional current starving technique, the proposed technique also improves the noise performance and settling speed of the amplifier. The results are compared with the conventional technique, in terms of gain, settling and noise performance. A comparison of FoM (MHz.pF/mA), with other amplifiers, is given at the end as well.

1. Introduction

Gain is an important parameter in amplifier design. In modern CMOS technologies, inherent gain of transistors is decreasing [1]. A variety of gain enhancement techniques have been proposed in the literature to enhance the gain of the amplifiers. Cascading more stages is usually not preferred as the stability is hard to guarantee in this case. This is why more than two stages, in an amplifier, are a rare sight. Cascoding is a valuable alternative to cascading [2], [5]. Cascoding enhances the gain without affecting the stability of the circuit significantly. Regulated cascode enhances the gain even more [6]. One drawback of cascoding is that it needs more head room, which may be an issue for low voltage applications.

Amplifying stages that have diode connected loads, sometimes use current starving technique to enhance the gain. Such an example is shown in Fig. 1 which shows one half of a differential pair, loaded by diode connected transistors. The voltage gain of such an amplifying stage is given by

$$A_{v\_DC} = -\frac{g_{m1}}{g_{m2}} \tag{1}$$

where g_{m1} is the transconductance of the input differential pair and g_{m2} is the transconductance of the load transistors. Clearly g_{m2} has to be decreased to get high gain. Increasing g_{m1}, to get more gain out of this stage, increases the power consumption.

Current mirror OTAs are more power efficient than conventional Miller compensated amplifiers [3]. However, current mirror OTA has relatively low voltage gain [3]. Current starving technique is often used in the design of current mirror based OTAs to increase the voltage gain [3]. A current mirror OTA that uses this technique is shown in Fig. 2. Transistor M_5 (M_6) is bigger than M_3 (M_4) by a certain factor, denoted by B_1. Increasing B_1 helps in improving the power efficiency; however, in reality there is always an optimum value, as shown in [2]. It is usually around 3–5. Gain bandwidth increases with increasing B_1, hence the power efficiency also increases with increase in B_1. It is worth mentioning that increasing B1 increases the silicon area which is a direct price to pay for gaining power efficiency.

The rest of the paper is organized as follows: Section 2 discusses the proposed technique, small signal analysis and the noise analysis, Section 3 presents the comparison of results of proposed and conventional technique. Sections 4 and 5 are about OTA design and conclusion of the paper respectively.

2. Proposed technique for gain enhancement

A current mirror based OTA is shown in Fig. 2. To enhance the gain of the OTA, a part of the current, coming out of the input differential pair, is taken away by current sources. As a result of less current flowing in to the diode connected transistors (M_3 and M_4), the transconductance of these transistors reduces. This results in better gain in the first stage and hence the overall gain improves as

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well. Common mode feedback circuit has been omitted in Fig. 2 for ease of drawing. $M_{7\text{-}8}$ are simply the output stage current sources.

The current I_s, taken away from diodes, flows in to the ground node, hence wasted. It is in fact possible to utilize this current for improving the gain further.

Consider the circuit shown in Fig. 3. This circuit makes use of the waste current, I_{11}, to enhance the gain further. Compared to a standard current mirror based OTA, shown in Fig. 2, an additional amplifying circuit (formed by M_9, M_{10}, M_{12} and M_{13}) is used. The additional circuit is shown, enclosed in dotted periphery in Fig. 3. The additional circuit achieves two purposes: first it biases the current sources (M_{11} and M_{14}) that take away the current of the diode connected devices (M_3 and M_4), and secondly it adds to the transconductance of input differential pair (M_1, M_2). As a result, the overall gain increases not only because current from diode connected devices (M_3, M_4) is taken away but also because of effectively more transconductance from the node *Vin* to node *Vp* (or *Vip* to *Vn*). The current consumed by M_{11} and M_{14} is the current that would normally go to ground. Currents in different branches are labeled in the Fig. 3.

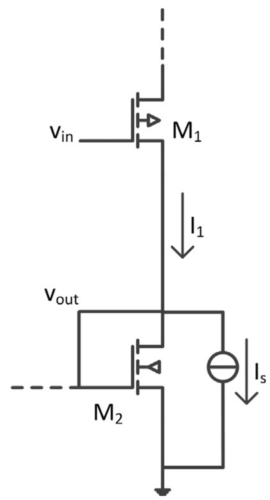

Fig. 1. An amplifying stage with diode as load, using current starving.

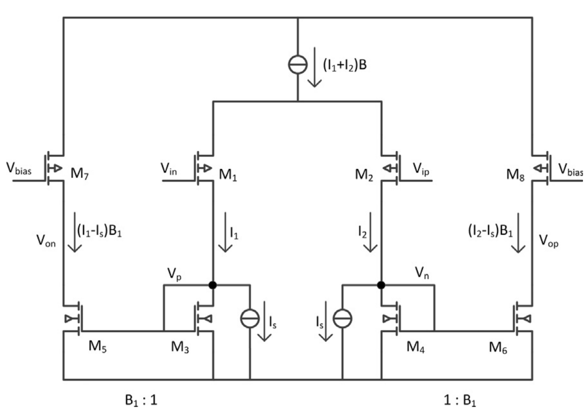

Fig. 2. Conventional current mirror OTA.

Compared to a standard current mirror based OTA, which employs current starving to increases the gain, I_9 and I_{10} appear to be contributing to additional power consumption. However, it is worth noting that the current consumed by M_9 and M_{10}, (I_9+I_{10}) is factor B_2 times smaller the current of M_{11} and M_{14} (the current to be taken away from diodes). Additionally, a bias current would be needed anyway for biasing the transistors that take away the current of diodes. Hence it can be said that the power consumption of auxiliary differential pair is not a penalty in terms of power consumption.

2.1. Small signal analysis

Having explained the basic principle of the new circuit, we now move to the small signal analysis of the proposed circuit. This will help us identify the dynamics of the amplifier that uses this technique for gain enhancement. An important definition, that will be used in this paper, is the current starving factor, denoted by 'S_f'. This is defined (referring to Fig. 3) as the ratio between the current flowing in M_{11} and the current flowing in M_1. In other words S_f defines how much of the actual current is diverted away from the diode connected device M_3 (M_4). S_f is given by:

$$Sf = \frac{I_{11}}{I_1} \tag{2}$$

where I_{11} is current flowing in M_{11} and I_1 is current flowing in M_1. To proceed with the small signal analysis, we assume that the amplifier, in Fig. 3, is loaded by a capacitance C_L. The output resistance of the second stage (formed by M_5 and M_7) is denoted by r_L. Consequently, the load pole is given by:

$$Z_L = \frac{r_L}{1+sC_L r_L} \tag{3}$$

For the small signal analysis, we will first calculate the transconductance expression, from input to output (from *Vin* to *Von*). Once

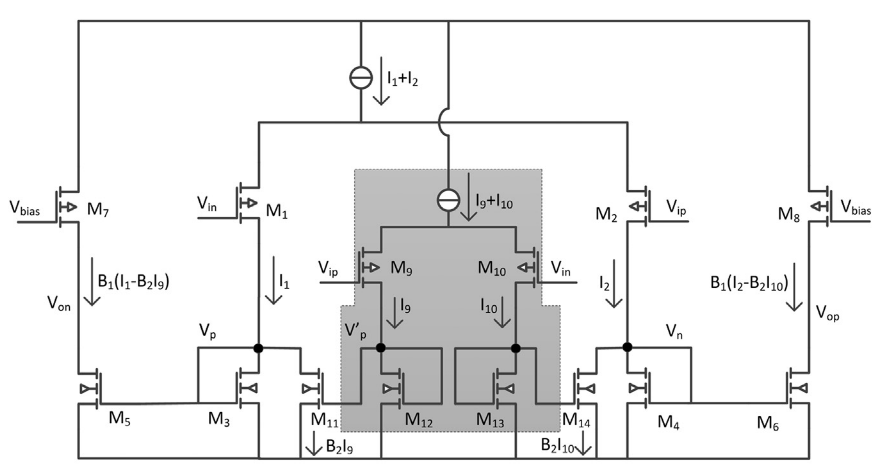

Fig. 3. Proposed current mirror OTA.