Microelectronics Journal 45 (2014) 50–58

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A wideband amplifier topology based on positive capacitive feedback

Francesco Centurelli *, Roberto Antonio Gualano, Alessandro Trifiletti

Dip. di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni, Università di Roma La Sapienza, Via Eudossiana, 18, 00184 Roma, Italy

ARTICLE INFO

Article history:
Received 6 May 2013
Received in revised form
25 September 2013
Accepted 30 September 2013
Available online 19 October 2013

Keywords:
Wideband amplifier
Bandwidth enhancement
Positive feedback
Optical communications

ABSTRACT

We propose a novel bandwidth expansion technique for cascode amplifiers, that exploits positive capacitive feedback (PCF) applied to the cascade of common base and common collector stages to increase the overall amplification at high frequencies. The resulting amplifier has a nearly unchanged input impedance, that we enhance introducing a second PCF loop. We present an ac model of the topology to better understand the behavior of the proposed technique and to compare it with other PCF-based amplifiers. Simulations, carried out using a 230 GHz-f_T SiGe technology, have shown a 40% bandwidth extension rate with respect to a simple cascode differential pair when a 50 Ω source resistance is used, and up to 59% for a 200 Ω source resistance. This is a 15–20% more than what can be achieved with other PCF techniques in the literature. The proposed topology is robust against process variations, and retains its advantages when accurate layout parasitics are taken into account.

1. Introduction

Wideband amplifiers are key building blocks for many electronic systems. For example, fiber optic communication applications require high gain amplifiers operating from dc to tens of GHz for both data amplification and clock distribution. The development of gain stages with bandwidths that are a significant fraction of the transition frequency of the devices is a key point to design low cost SiGe-based integrated systems for high speed optical communications using presently available technologies, and bandwidth expansion techniques are required to achieve this goal.

Negative feedback is not a solution for these applications, since the high gain and large bandwidth required would make a too low loop gain available; moreover, it could be difficult to achieve enough phase margin. Therefore many alternative techniques have been proposed to increase the bandwidth of the basic buffered differential pair stage. The TAS–TIS topology [1,2], based on the approach proposed by Cherry and Hooper in [3], exploits the impedance mismatch of cascaded transadmittance (TAS) and transimpedance (TIS) stages in order to minimize the loading effect at interface nodes. The crucial point of TAS–TIS design is the trade-off between bandwidth and peaking: the TIS circuit, typically a shunt–shunt feedback stage, must be properly designed in order to avoid large peaking of the frequency response, that could result in low fidelity of the amplifier response and eye closing when used in pulse applications. Another widely used topology is the shunt-peaked amplifier [4,5], which exploits an inductor in series with the load resistor of a common emitter or cascode so that the overall load impedance can remain approximately constant or even increase at high frequencies, in order to equalize the voltage gain. The main drawback of this technique is the large chip area occupied by the inductors. This problem can be solved by using active inductors [6,7], however a large dc voltage drop is required for this solution and additional transistors could introduce linearity and noise limitations. Another wideband topology proposed by Wakimoto [8,9] exploits an active compensation circuit in order to cancel parasitic capacitances at input or output nodes of the amplifier. The compensation circuit is based on an active feedback network, thus requiring additional transistors. This topology could result in constraints on the minimum supply voltage that could limit its application in a low voltage environment. Moreover, when high speed devices are used, input and output poles become comparable, so Wakimoto's approach results less effective. Several bandwidth expansion techniques are based on a positive capacitive feedback (PCF) approach: the feedback loop is open at low frequencies, thus dc gain is not affected, whereas at high frequencies, where gain begins to drop, positive feedback equalizes the frequency response, compensating the drop with peaking and thus expanding the overall bandwidth. This idea has been applied as C_μ-compensation in [10], with the feedback capacitor chosen to cancel the C_μ of the transistor, and then in wideband stages as transimpedance feedback in [11] and as voltage feedback [12] by some of the authors. In these more general cases, the feedback capacitance is used to set the poles of a feedback loop, which may or may not include the output emitter follower, in the required positions to achieve large bandwidth and

* Corresponding author. Tel.: +39 06 44585787; fax: +39 06 44585918.
E-mail addresses: centurelli@die.uniroma1.it, fcentur@ieee.org (F. Centurelli), gualano@die.uniroma1.it (R.A. Gualano), trifiletti@die.uniroma1.it (A. Trifiletti).

0026-2692/$ - see front matter © 2013 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.mejo.2013.09.013

negligible peaking [13,14]. Moreover no additional power and negligible supplementary chip-area are required, therefore making these techniques largely used.

In this paper we propose a novel PCF-based bandwidth expansion technique applied to a cascode differential pair (CDP), that offers a better trade-off between bandwidth and peaking with respect to similar techniques in the literature. The proposed topology is presented in Section 2, and Section 3 discusses its properties using feedback theory. Section 4 presents a comparison with other bandwidth expansion techniques, and in particular with the Vadipour technique applied to a cascode differential pair. Simulation results are reported in Section 5, and in Section 6 conclusions are drawn.

2. Topology description

As the transition frequency of recent high-speed SiGe HBTs rises, the breakdown voltage of the devices is getting lower and lower [15]. This not only imposes a limitation in terms of voltage swing, but also introduces some biasing issues in dc-coupled circuit design. If we consider the basic gain stage, composed by a simple differential pair with an output emitter follower as voltage buffer, cascading dc-coupled stages requires that the output dc level of each stage has to be compatible with the input dc level of the following one. For a cascade of identical stages, this implies that $V_{OUT}=V_{IN}$ is required. This condition results to be satisfied for:

$$V_{CE}^{DP}=V_{BE}^{CC}+V_{BE}^{DP} \tag{1}$$

where V_{CE}^{DP} and V_{BE}^{DP} are the collector-emitter and the base-emitter dc voltages of the differential pair transistors and V_{BE}^{CC} is the base-emitter dc voltage of the common collector transistor. In case of very high speed HBT devices, (1) could result in a collector-emitter voltage higher than the breakdown voltage (e.g. $V_{BE}=0.85$ V and breakdown voltage $BV_{CE}=1.2$ V), thus requiring the use of a cascode configuration. This also reduces the input capacitance by minimizing the Miller effect, improving the bandwidth.

However a more significant bandwidth enhancement can be achieved through the use of PCF techniques. PCF techniques presented so far were applied to standard differential pairs, but they can be easily applied to cascode structures. The solution in [12] applied a voltage feedback and required emitter degeneration, thus making the technique not suitable for high gain amplifier design. The topology in [11] exploited a transimpedance feedback closed on the input node, making the loop gain dependent on the source impedance.

The use of a cascode configuration provides a low impedance node where a feedback loop can be closed with a gain that is independent from the input load condition. This results in the wideband gain stage topology shown in Fig. 1. The circuit can be modeled (Fig. 2) as a transadmittance stage (TAS), given by Q_1, loaded by a transimpedance stage (TIS), composed by Q_2 and Q_3 with a positive capacitive feedback given by C, therefore exploiting the TAS–TIS principle. Notice that the topology doesn't need cross-coupled capacitors, thus avoiding layout complexity. Since the transconductor is placed out of the loop, the input pole, which stands at high frequencies because of the use of the cascode, turns out to be at a first approximation independent from C. This pole therefore isn't affected by feedback, and this also contributes to a larger bandwidth expansion than in [11], as will be shown in the next sections.

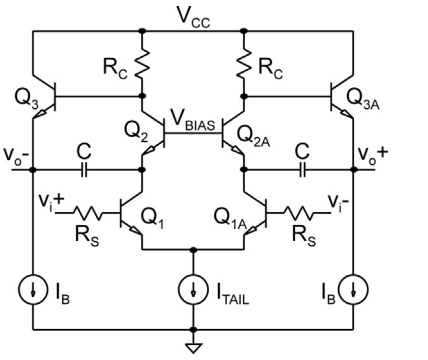

Fig. 1. Proposed topology of wideband amplifier.

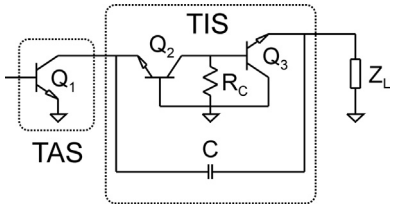

Fig. 2. Block scheme of the proposed topology.

3. Circuit analysis

We have developed a small signal model of the proposed PCF topology, based on feedback theory, in order to better understand its properties and to allow comparison with different PCF based topologies.

Fig. 3 shows the open loop differential half circuit of the transimpedance stage (Q_2–Q_3), including the loading effect of the feedback network (capacitor C). The transconductance stage Q_1 has been modeled by its Norton equivalent, resulting in a transconductance gain

$$G_{mo}=\frac{-g_{m1}r_{\pi1}}{R_S+r_{b1}+r_{\pi1}}\frac{1}{1+sC_{IN}(R_S+r_{b1})\|r_{\pi1}} \tag{2}$$

and an output admittance

$$Y_o=G_o+sC_o=1/r_{o1}+s(2C_{\mu1}+C_{P1}) \tag{3}$$

where R_S is the source resistance, $C_{IN}=C_{\pi1}+2C_{\mu1}$ and C_{P1} is the parasitic capacitance at the output of the transconductor, including the collector-to-substrate capacitance of Q_1 (Miller approximation has been exploited). C_C in Fig. 3 includes all the capacitances at the collector of Q_2 ($C_{\mu2}$, $C_{\mu3}$ and parasitics), C_L includes the load capacitance and output parasitics, and R_L includes the output resistances of Q_3 and of the current generator I_B, and the load resistance (we are neglecting the base resistances of Q_2 and Q_3).

The open loop transimpedance gain can be written as:

$$TZ_{OL}=\frac{1}{Y_A+sC+Y_i}A_VA_B \tag{4}$$

where $Y_A=Y_o+Y_{\pi2}$,

$$Y_i=g_{m2}+(1-A_V)/r_{o2} \tag{5}$$

is the admittance seen into the emitter of Q_2 as shown in Fig. 3,

$$A_V=\frac{(g_{m2}+G_o)(g_{m3}+Y_{\pi3}+1/R_L+s(C_L+C))}{Y_{\pi3}(1/R_L+s(C_L+C))+(1/R_C+sC_C)(g_{m3}+Y_{\pi3}+1/R_L+s(C_L+C))} \tag{6}$$

is the voltage gain of the common base stage, and

$$A_B=\frac{g_{m3}+Y_{\pi3}}{g_{m3}+Y_{\pi3}+1/R_L+s(C_L+C)} \tag{7}$$

is the voltage gain of the emitter follower. Eqs. (4)–(7) can be rearranged by assuming $g_{m2,3}\gg 1/r_{o2,3}$, $g_{m2,3}\gg 1/r_{\pi2,3}$, $g_{m2}\gg G_o$,