



A 33 mW 12.5 Gbps BiCMOS transmitter for high speed backplane applications

Khaldoon Abugharbieh^{a,*}, Yongseon Koh^b, Shoba Krishnan^c, Jitendra Mohan^b

^a Princess Sumaya University for Technology, Amman, Jordan

^b Texas Instruments, Santa Clara, CA, USA

^c Santa Clara University, Santa Clara, CA, USA

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ABSTRACT

This paper describes a 12.5 Gbps voltage mode transmitter with a high speed signal conditioning capability. Using a linear equalizer that is followed by a power efficient output stage, the transmitter achieves pre-emphasis at very low power consumption. In measurements, the transmitter can reliably transmit a 12.5 Gbps PRBS7 signal through a lossy 14 in. FR4 stripline commonly used in backplanes. It achieves a peak to peak jitter of 24 ps, a differential eye opening amplitude of 120 mV, and a maximum common mode ripple of 40 mV. The proposed topology consumes 33 mW at-speed power which includes both the output stage and the linear equalizer. It also passes 8KV HBM ESD testing without compromising the high speed capability. The transmitter is fabricated in a 130 nm BiCMOS technology with 100 GHz maximum f_t and packaged in a commercial leadless leadframe package.

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1. Introduction

Fig. 1 shows a model of a data transfer system with a transmitter, a receiver and a lossy transmission channel. When a high speed signal is traveling through a long channel, the signal will degrade due to the channel's bandwidth limitations. The channel's frequency response can be modeled as a low pass transfer function as shown in Fig. 1 [1–3].

When the data rate is higher than the bandwidth of the channel, signal attenuation causes the binary data not to transition completely within a symbol interval. As a result, the binary data will spread into the adjacent symbols, which is known as inter-symbol interference or ISI [4–7]. To reduce the effect of ISI, the signal is often given extra amplitude during transition which amounts to a high frequency boost in the frequency domain [8]. This process is called pre-emphasis or signal equalization which has a frequency characteristic also shown in Fig. 1. The transmitter acts as a pre-equalizer that boosts the high frequency component of the signal which gets attenuated through the channel. The amplitude and duration of the boost are set to offset the signal loss in the channel. The longer the channel is, the higher the boost needs to be. Generally, the duration of the boost is set less than or equal to one data interval.

To achieve signal equalization, CML based topologies are commonly used. Fig. 2a shows a typical CML driver without signal conditioning, and Fig. 2b shows a CML driver when signal equalization is used. The equalization is done in the output stage of the driver. The swing depends on the data pattern. For example, if the data is changing, like pattern 010, the amplitude swing is maximum as in Eq. (1). However, when the data is steady, like pattern 111, the amplitude swing is minimum. While CML topologies are common, they are not power efficient. As in Eqs. (1) and (2), the output stage consumes a current that is proportional to four times the load current which does not include the pre-driver current.

$$V_{o,cml_max} = R_L \times \left(\frac{I_{tail}}{4} \right) \quad (1)$$

$$V_{o,cml_min} = R_L \left(\frac{I_{main}}{4} - \frac{I_{pre}}{4} - \frac{I_{post}}{4} \right) = R_L \left(\frac{I_{tail}}{4} - \frac{I_{pre}}{2} - \frac{I_{post}}{2} \right) \quad (2)$$

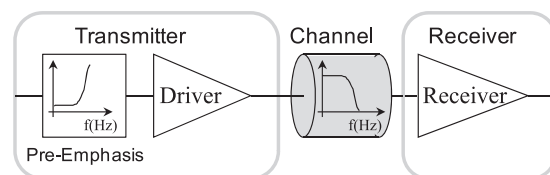


Fig. 1. Model of a data transfer system.

* Corresponding author. Tel.: +962 6 5678 014.

E-mail address: k_abugharbieh@yahoo.com (K. Abugharbieh).

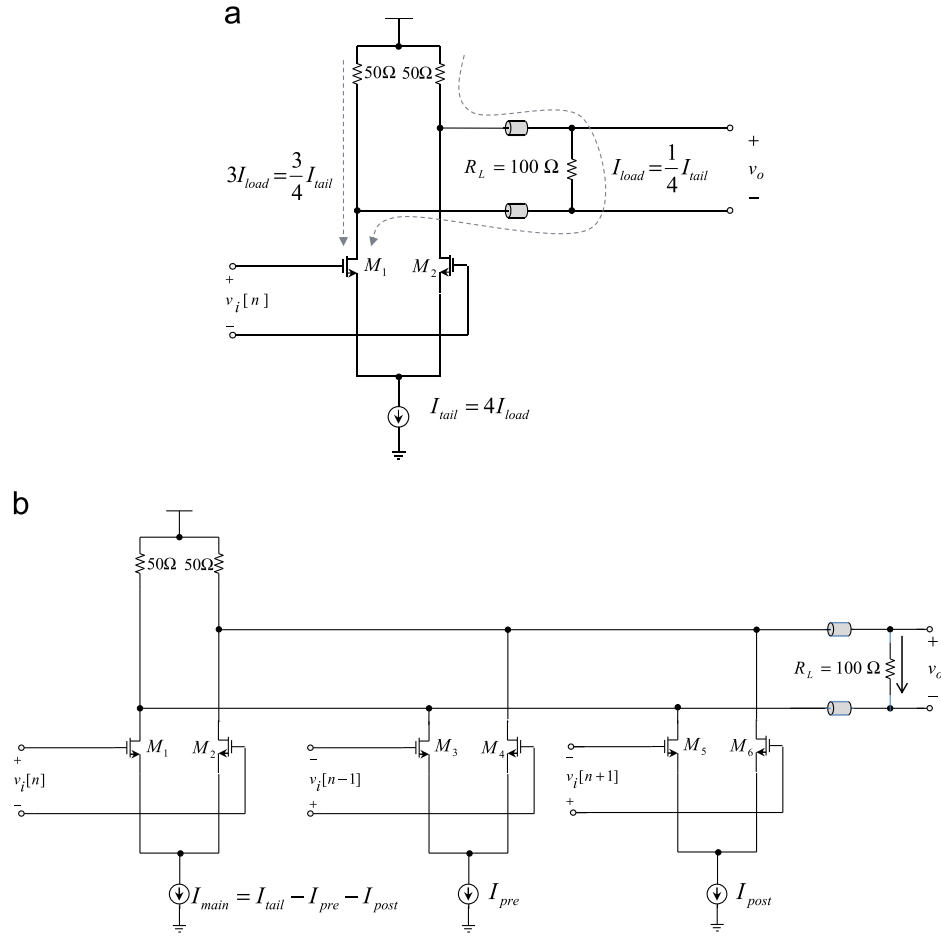


Fig. 2. (a) Typical CML driver and (b) CML driver with signal conditioning.

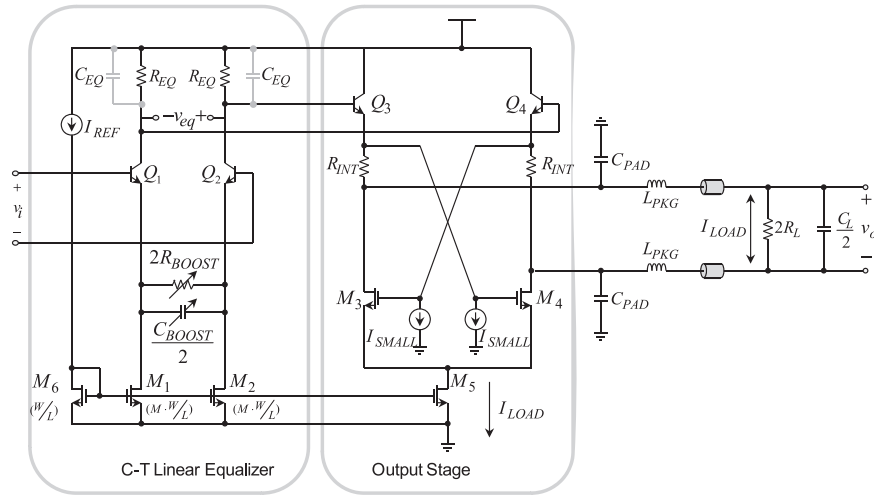


Fig. 3. Simplified schematic for new voltage mode transmitter with pre-emphasis.

The work presented in this paper will offer a novel way to achieve signal equalization in the transmitter at significantly lower power consumption than commonly used CML based topologies [9–12]. Section 2 will explain the new topology details along with some simulations results. Section 3 will present silicon measurements in addition to comparisons with other published work. Section 4 presents a conclusion which summarizes the new topology performance.

2. Pre-emphasis transmitter topology

Fig. 3 shows a schematic of the new voltage mode transmitter with differential output voltage and pre-emphasis. The circuit consists of a linear equalizer and an output stage. The output stage can achieve good line impedance matching while keeping the power consumption very low using a positive feedback technique [13]. Pre-emphasis capability is achieved in the linear

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