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Internally compensated LDO regulator based on the cascoded FVF

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ABSTRACT

In this paper, an internally compensated low dropout (LDO) voltage regulator based on the Flipped Voltage Follower (FVF) is proposed. By means of capacitive coupling and dynamic biasing, the transient response to both load and line variations is enhanced. The proposed circuit has been designed and fabricated in a standard 0.5 μm CMOS technology. Experimental results show that the proposed circuit features a line and a load regulation of 132.04 μV/V and 153.53 μV/mA, respectively. Moreover, the output voltage spikes are kept under 150 mV for a 2 V-to-5 V supply variation and for 1 mA-to-100 mA load variation, both in 1 μs.

1. Introduction

Power management in integrated circuits (ICs) has become a key research area in both, battery powered and energy harvesting applications, as a consequence of the limited amount of available energy. Power management goes beyond turning off a part of the system when it is not required. It is critical in autonomous devices such as those used in wearable electronics and wireless sensor networks, where the source of energy suffers from extremely high variations. In this sense, low dropout (LDO) regulators have shown to be essential blocks as they generate a regulated voltage with low quiescent consumption under large variations of load and input voltage.

A LDO is a linear voltage regulator that operates with a high efficiency thanks to a small input–output voltage difference. An internal compensation of LDOs is usually preferred, as it does not require external capacitors, reducing size and cost. In the last few years, a number of different techniques have been proposed to increase the stability of internally compensated LDOs and to enhance their transient response. Miller compensation results in highly stable LDOs with fast transient response, however, the required area of the Miller capacitor is usually significant in comparison with the total area of the chip. In [1,2], current amplifier Miller compensation is used, reducing the total compensation capacitance but increasing the power consumption and the complexity of the design. The so-called damping-factor-control (DFC) technique, which was initially proposed to compensate multistage amplifiers driving heavy capacitive loads, has been recently used to compensate a LDO [3,4]. The DFC block allows controlling the damping factor of the complex pole pairs of the system avoiding the peak of resonance, which is responsible for instability.

On the other hand, different techniques have been proposed in the literature to improve the transient response of LDOs. In [5] and [6], a high slew-rate push–pull output amplifier was used to charge/discharge rapidly the pass transistor gate capacitance resulting in a small settling time under variations of the load current. However, no enhancement is achieved in the transient response for input voltage (V_{IN}) variations.

Another solution uses a fast self-reacting loop that allows rapidly drive the power transistor to regulate the output voltage [7]. In this case, three different paths are added to vary the voltage at the gate of the pass transistor when I_{LOAD} changes. In [8] and [9] the Flipped Voltage Follower (FVF) [10,11] was identified as the core cell for LDO design. The good performances of this cell as a current buffer and its low output impedance make it a highly efficient LDO regulator according to load regulation. However, its response due to input voltage variations is limited by the biasing currents, which are responsible for the charge/discharge of the gate parasitic capacitance of the pass transistor. Thus, there is a trade-off between power consumption and transient response.

Further work on this structure has been done creating a path that couples the changes variations in the output voltage V_{OUT} to the gate of the pass transistor [12]. This technique can be used to improve both, the line and load transient responses, and can be implemented in a simple way by means of RC coupling.

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In this paper, an FVF-based LDO regulator, which uses the cascoded version of the FVF, is proposed which improves line regulation and transient behavior of existing implementations based on this cell. The proposed regulator uses RC coupling to solve the transient problems of the circuits in [8] and [9] for input voltage variations without a significant increase in the quiescent power consumption. The organization of this paper is as follows: Section 2 describes the structure and principle of operation of the proposed structure; Section 3 analyses its stability; and in Section 4, measurements of the proposed LDO regulator designed in a standard 0.5 μm CMOS technology are presented. Finally, some conclusions are drawn in Section 5.

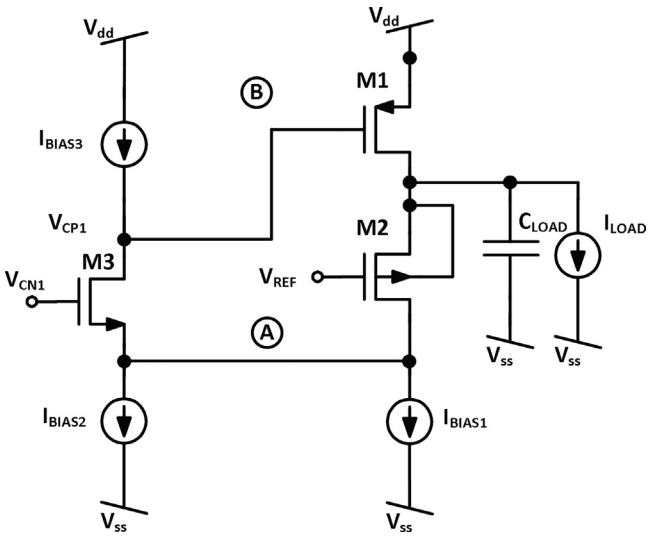

Fig. 1. Structure of the cascoded FVF.

2. Structure and principle of operation

The proposed structure is based on the cascoded FVF (Fig. 1), whose core consists of transistors M1–M3. Specifically, M1 is the pass transistor and it is responsible for providing the current to the load (I_{LOAD}). M2 acts as an error amplifier, which compares the output of the LDO with the reference voltage (V_{REF}). Node A tends to follow the variations in V_{OUT} because of the current flowing through transistor M2 is fixed by I_{BIAS1}. As a result, these variations are amplified by the transconductance of the M2 and they are coupled to the node B. In this way, the parasitic capacitor of the pass transistor gate is charged or discharged to cope with changes in I_{LOAD}.

As stated in the introduction, the main disadvantage of the structure in Fig. 1 is its slow transient response. This is limited by biasing currents I_{BIAS2} and I_{BIAS3} which are responsible for charging/discharging the parasitic capacitance at node B. This limitation leads to large output variations. In order to improve the transient response of the circuit, I_{BIAS2} and I_{BIAS3} are replaced by dynamic current sources dependant on the input and output voltages as shown in Fig. 2a. For this circuit, if voltage V_{IN} rises, node X instantaneously tends to increase its voltage, producing an increase of the current in M13 and, hence, in I_{BIAS2} which allows a fast charge of the gate parasitic capacitance of M1. In addition, the output voltage is coupled to magnify this effect taking advantage

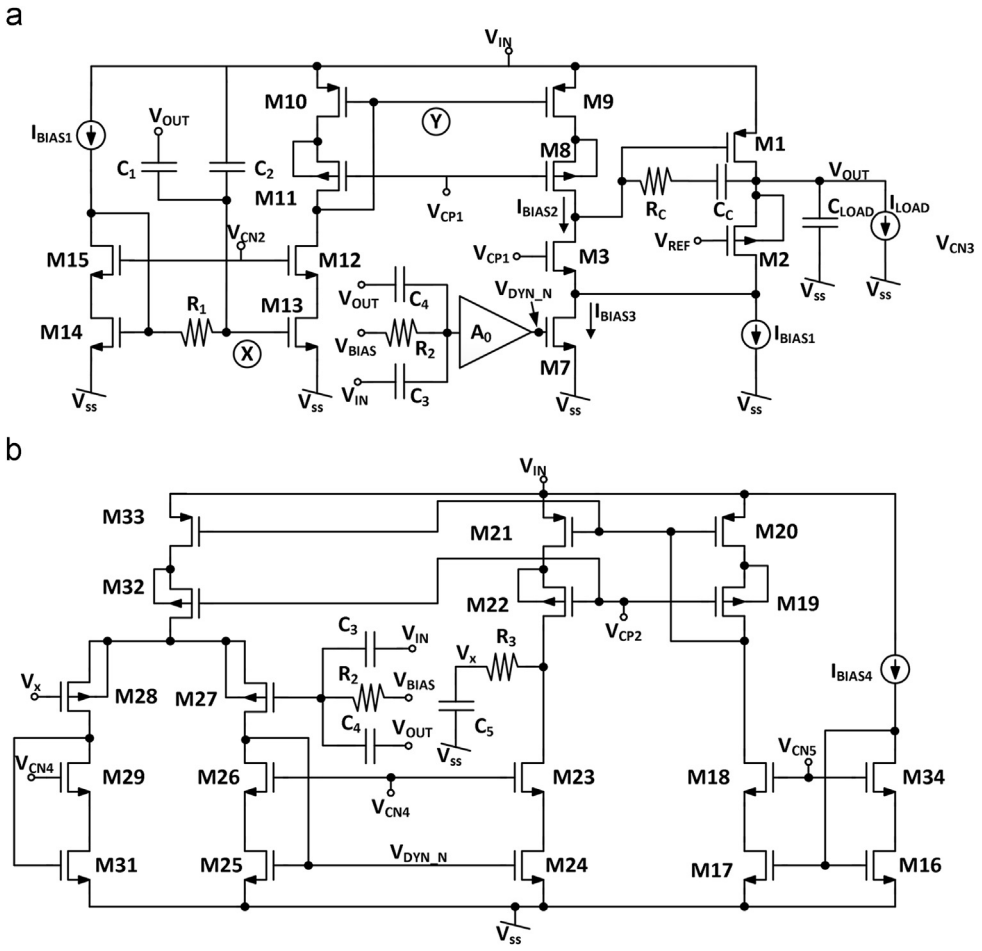

Fig. 2. Structure of the proposed LDO. (a) Core of circuit. (b) Differential amplifier.