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Low power low noise high speed tunable CMOS radiation detection system

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ABSTRACT

This paper presents a design of low power and low noise, high speed readout front-end system for semiconductor detectors. The architecture comprises a folded cascode charge sensitive amplifier with gain enhancement, a pole-zero cancellation circuit and a complex shaper circuit with Gm-C topology. A local feedback amplifier based on a wide swing gain boosting scheme with dc level shifting has been used. The system has been fabricated in a 0.13-μm CMOS technology with a single 1.2-V supply voltage. Experimental results show the flexibility of the system where the key parameters, such as decay time, charge gain and peaking time can be tuned. For a nominal peaking time of 150 ns the power consumption of the entire channel is less than 5 mW. A power consumption-low noise tradeoff will be considered to match a detector capacitance of 5 pF. The output pulse has a peak amplitude of 200 mV for a charge of 10 fC from the detector and achieves a linearity better than 1% up to an input charge range of 12 fC.

1. Introduction

The development of low noise low power readout front-end systems is of great interest today in several applications. Several sensors produce electrical charge in response to an external physical magnitude, such as piezoelectric sensors, photodetectors, pyroelectric sensors, particle detectors, and radiation detectors [1]. In particular, semiconductor detectors are extensively used for photon-counting imaging systems in medicine and for charged particle detection in nuclear physics applications. They are reverse-biased diodes that releases charge towards its electrodes when exposed to radiation. The energy deposited in these detectors is converted to an electric signal. To measure the deposited energy, which is proportional to the current pulse amplitude, a readout electronics is required. The analog front-end system is a conditioning channel that processes the information coming from the sensor and delivers it in a suitable form for further analog processing or digitalization. The trend to integrate the full electronic processing channel has become a priority due to high density and increased number of channels demanding low power, low noise and small area as well as the capability to include analog and digital circuits on the same chip. This approach replaces the conventional discrete and hybrid electronics [2–4].

The scaling down of the technology allows high speed front-end systems with small die area at the cost of low supply voltage and noise constraints [5]. The low supply voltage complicates the design requiring very efficient topologies. The design of operational amplifiers, which are the most important block in the front-end electronics, presents the additional difficulty of providing high gain and high output swing combining low-voltage operation with high power efficiency. Currently, gain enhancement techniques in combination with low voltage techniques are required to overcome the low intrinsic gain limitation in submicron technologies. Cascade structures that boost the gain with several amplifying stages need frequency compensation increasing the power consumption and limiting the bandwidth. The usual way to boost the gain is through cascode transistors but the design requires small overdrive voltages due to the output swing limitation.

This paper addresses the design of a readout front-end system for the radiation detection using silicon detectors. The aim of the work is to preserve or even to increase the system performance under low supply voltage operating conditions, optimum low power dissipation, and low noise. The use of a modern CMOS process requires a careful design where the analog transistor properties are worsened. This work uses a gain-boosting technique based on a local feedback amplifier with a wide-swing approaching.

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The paper is organized as follows: An overview of the designed readout front-end system is given in Section 2. Section 3 discusses design considerations related to key parameters. Section 4 deals with the topology of the charge sensitive amplifier and the gain boosting scheme used. Section 5 presents the shaping circuit and simulation and experimental results are given in Section 6. Section 7 contains a summary.

2. Architecture of the designed front-end system

Radiation events hit a reversely biased semiconductor detector and the number of electron-hole pairs released is proportional to the energy of detected particles. The detector delivers a charge that must be amplified and shaped. Fig. 1(a) shows the architecture of the readout front-end channel designed in this paper for the radiation detection using silicon detectors. The system consists of a folded-cascode charge sensitive amplifier (CSA) with gain-boosting technique, a pole-zero cancellation circuit to eliminate undershoot, a shaper amplifier, and some integrators using Gm-C filter topology. The charge generated in the detector is fed to a charge sensitive amplifier (CSA) where the incoming current pulses are integrated by a feedback capacitor C_F and converted into voltage pulses. This kind of amplifier is commonly used due to the gain is insensitive to the detector capacitance C_{det} [6–8]. The CSA's output is a voltage step with amplitude proportional to the charge generated in the detector. This voltage pulse then slowly discharges by the feedback resistance R_F connected in parallel to C_F. The decay time must be adjusted to achieve a fast return to zero in order to prevent the pile-up of subsequent incoming current pulses in case of high rate experiments.

The voltage pulse is then amplified and shaped according to the time requirements of the application by a pulse shaping amplifier (shaper). The shaper also improves the signal to noise ratio of the signal by filtering the noise. It consists of a high pass section followed by several integrators. The CSA is dc coupled to the shaper. A pole-zero cancellation (PZC) circuit avoids the undershoot at the output of the shaper produced by the feedback pole of the CSA.

The back-end electronics processes the shaper's output signal in different ways depending on specific applications as shown in Fig. 1(b). The three main blocks that can be used for measuring the shaper's output are: a discriminator that uses a comparator to detect the signal amplitude and compares it with a threshold (counting), an analog to digital converter to measure the amplitude of the signal corresponding to each individual impinging particle (energy spectroscopy), or a time to digital converter for timing measurements (timing spectroscopy).The acquired information can be stored in the chip or sent out from it.

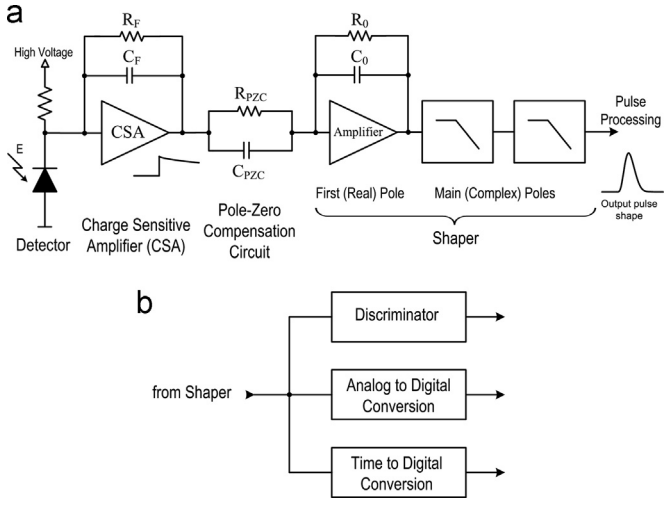

Fig. 1. (a) Architecture of the designed readout front-end system. (b) Back-end electronics.

3. Design considerations

The noise limit to the resolution of a radiation detection system is typically expressed in terms of equivalent noise charge (ENC). The ENC corresponds to the charge that must be delivered to the front-end in order to achieve an output signal to noise ratio equal to the unity. An equivalent definition for ENC is the ratio of total integrated rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge, ENC$=v_{no,rms}/V_{out,max}$, yielding [5]

$$\mathrm{ENC}^2 = \frac{\int_0^\infty |v_{no}(j2\pi f)|^2 |H(j2\pi f)|^2 \, df}{qA^n n^n / C_F n! e^n} \tag{1}$$

where $v_{no,rms}$ is the total rms noise and $H(j2\pi f)$ is the transfer function of the shaper. In addition, n is the order of the shaper/filter, A is the dc gain of the integrators of shaper, and C_F is the feedback capacitor of the CSA. The final equation after solving is given as follows:

$$\mathrm{ENC}^2 = 4k_B T \frac{\gamma}{g_m} \frac{C_T^2 B((3/2), n-(1/2))n}{q^2 4\pi t_p} \left(\frac{n!^2 e^{2n}}{n^{2n}}\right) + \frac{K_f C_T^2}{C_{ox}^2 WLq^2 2n} \left(\frac{n!^2 e^{2n}}{n^{2n}}\right) \tag{2}$$

The first term is the contribution of the thermal noise and the second term is the flicker noise contribution. The meaning of the main parameters is as follows: k_B is the Boltzmann constant, T is temperature, g_m is the input transistor transconductance of the CSA, C_{ox} is the gate oxide capacitance per area, W and L are the width and length of the input transistor, K_f is the flicker noise coefficient, C_T is the total input capacitance consisting of detector, feedback and input transistor capacitances, B is the beta function defined in [5], t_p is peaking time, i.e. a measure of the speed of the detection system. Finally, $\gamma = 2/3$ for long channel MOS transistors and is approximately 1.5–2 in submicron technologies. There is another thermal noise source associated with the feedback resistance R_F. This noise contribution is inversely proportional to the value of the feedback resistance and proportional to the peaking time. The decay time of the CSA's output is proportional to R_F providing a tradeoff between noise and pile-up (overlap between successive input pulses).

Now that detector trends force a strong power constraint on the electronics, it is important to clarify the tradeoff between noise and power dissipation. The readout front-end system noise performance is strongly dependent on the input MOS transistor of the charge sensitive amplifier related to type, size and biasing. In a properly designed front-end the resolution should be limited by the noise of the CSA input transistor. Regarding the dominance of thermal and flicker noise in (2) for the input transistor, it is anticipated here that the thermal noise is the dominant noise source due to the low peaking time (150 ns). The peaking time specification defines the bandwidth of the shaper, and hence, determines the dominance of thermal or flicker noise. Therefore, in order to reduce the thermal noise, the transconductance g_m of the CSA's input transistor has to be increased, and g_m is directly related to the power consumption and the aspect ratio W/L. The flicker noise is inverse proportional to the gate area of the input transistor and strongly dependent on the technology process. Moreover, a p-channel MOS input transistor has been chosen