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Low-leakage soft error tolerant dual-port SRAM cells for cache memory applications

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ABSTRACT

As transistor dimensions are reduced due to technological advances, the area constraint is becoming less restrictive, but soft error rate, leakage current, and process variation are drastically increased. Therefore, in nano-scaled CMOS technology, soft error rate, leakage current and process variation are the most important issues in designing embedded cache memory. To overcome these challenges, and based on the observation that cache-resident memory values of ordinary programs exhibit a strong bias towards zero, this paper deals with new low leakage, hardened, and read-static-noise-margin-free SRAM memory cells for nano-scaled CMOS technology. These cells are completely hardened and cannot flip from particle strikes at the sensitive cell nodes. Furthermore, these new SRAM cells have free read-static-noise-margin, such that transistor mismatching, due to process variation, cannot destroy stored-data of the cells during read operation. The new cells retain their data with leakage currents and positive feedback without a refresh cycle. The basic version of new cells consists of one write port with differential write-bit-lines and one read port with differential read-bit-lines, and the improved-leakage version of new cells consists of one write port with differential write-bit-lines and one read port with a single read-bit-line. Simulation results show that the proposed cells in this work correctly operate during their read, write, and idle cycles even while considering the process variation in 22-nm technology. In the worst case, our cells have 40% lower average leakage current in comparison with conventional 6T SRAM cell without any performance degradation. Also, our cells are hardened. Thus, they have zero soft error rate.

1. Introduction

Devices in CMOS technology have been scaled down aggressively with each technology generation to achieve a higher integration density and performance [1]. However, the leakage current has increased drastically with technology scaling and has become a major contributor to the total IC power [1]. Furthermore, as the feature sizes of devices and the supply voltage in CMOS technology were scaled down, the probability of soft errors increased. Soft errors are radiation-induced faults that occur because of a particle hit, either by an alpha particle from impurities in the packaging material or a neutron from cosmic rays [2]. Moreover, as the feature size of devices is scaled down, the random variations in process parameters have emerged as a major design challenge in circuit design [3]. These random variations of device parameters in nano-scaled CMOS technologies include random variations in channel length, channel width, oxide thickness, threshold voltage, etc. [3]. These random parameter variations result in significant variations in the characteristic of digital circuits [3].

The on-chip caches can effectively reduce the speed gap between the processor and main memory; almost modern microprocessors employ them to boost system performance. These on-chip caches are usually implemented using arrays of SRAM cells. A six-transistor SRAM cell is conventionally used as the memory cell [3]. As mentioned above, as CMOS technology scaled down, total leakage current of a chip increased. Furthermore, the total leakage current of a chip is proportional to the number of chip transistors. Since the cache memory includes a large number of transistors of modern microprocessor chips, the SRAM cell leakage has also become a more significant component of total chip leakage in scaled CMOS technology. In addition, in scaled CMOS technology supply voltage and nodal capacitance is reduced. Thus, low energy particles can flip SRAM cells, making cache memory cells more sensitive to atmospheric neutrons and alpha particles. Furthermore, the mismatch in the strength between transistors of conventional SRAM cell due to process variations can results in failure during read operation (flipping of the cell

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data while reading) [3], especially at low-V_{DD} level [4]. Therefore, conventional six-transistor SRAM cell (CV 6T SRAM cell) has a poor stability at very small feature sizes. Thus, leakage current, read-static-noise-margin, and soft error rate of SRAM cell are three important parameters in designing SRAM cells for cache memory in nano-scaled CMOS technology.

In response to these challenges, our objective is to develop hardened read static-noise-margin-free SRAM cells with dual threshold voltage transistor to reduce the leakage current of cell without any performance degradation. The rest of this paper is organized as follows. First, Section 2 describes our previous work and in this section based on our previous work, we propose new SRAM cells for cache memory applications. Then, a particle strike to new SRAM cells is investigated in Section 3. Next, in Section 4, the leakage current of new SRAM cells is investigated. Section 5 describes the concept of read-static-noise-margin and cell current, and deals with designing different read-static-noise-margin free SRAM cell techniques. Section 6 deals with the read delay of new SRAM cells. Process variation effects on new SRAM cells and CV 6T SRAM cell are investigated in Section 7. Next, in Section 8, layout and area of new SRAM cells are investigated. Section 9 deals with cache architecture based on the new cells. In Section 10, there are descriptions and discussions about previous related works. Then, Section 11 shows experimental results. Section 12 deals with a comparison with other previous related works. Finally, we summarize the key results in Section 13.

2. Our previous work and new SRAM cells

Fig. 1 shows an SRAM cell which is presented in our previous work [5]. In this SRAM cell for reducing charge sharing [6], same potential nodes (ST and N1 or STB and N2) are separated from each other [5]. Table 1 lists the sizes of transistors and threshold voltage level in reduced-charge-sharing SRAM cell (RCS-SRAM cell) presented in our previous work [5]. As shown in [5], RCS SRAM cell is completely hardened and cannot flip from particle strikes at the sensitive cell nodes. This SRAM cell can be used as configuration memory cell in configurable FPGA resources [5] and the desired data can be written into cell by using differential write port (WBL and WBLB in Fig. 1). However, RCS SRAM cell has the following limitations:

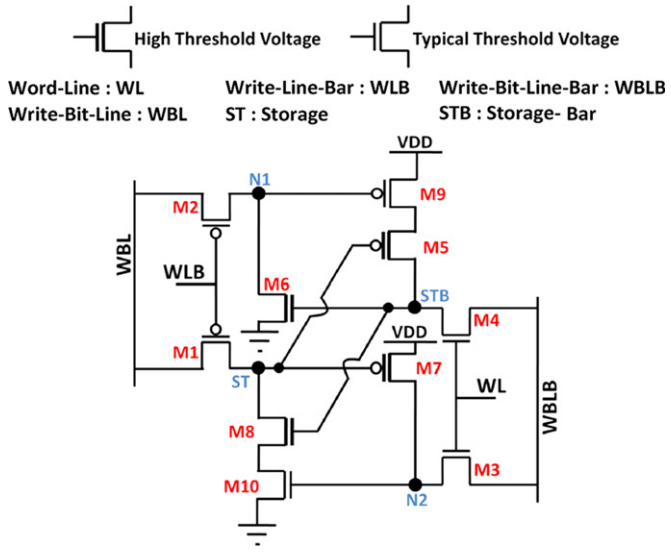

Fig. 1. Reduced-charge-sharing SRAM cell (RCS SRAM cell) to reduce the possibility of upsets due to charge sharing by separating same potential adjacent nodes [5]. Word-Line: WL Write-Line-Bar: WLB Write-Bit-Line-Bar: WBLB Write-Bit-Line: WBL ST: Storage STB: Storage-Bar.

Table 1
Transistor size (W/L) and threshold voltage level in reduced-charge-sharing SRAM cell [5].

Transistor	Size (W/L)	V_T	Transistor	Size (W/L)	V_T
M1	88 nm/22 nm	Typical	**M6**	44 nm/22 nm	High
M2	44 nm/22 nm	Typical	**M7**	44 nm/22 nm	High
M3	44 nm/22 nm	Typical	**M8**	44 nm/22 nm	High
M4	88 nm/22 nm	Typical	**M9**	44 nm/22 nm	Typical
M5	44 nm/22 nm	High	**M10**	44 nm/22 nm	Typical

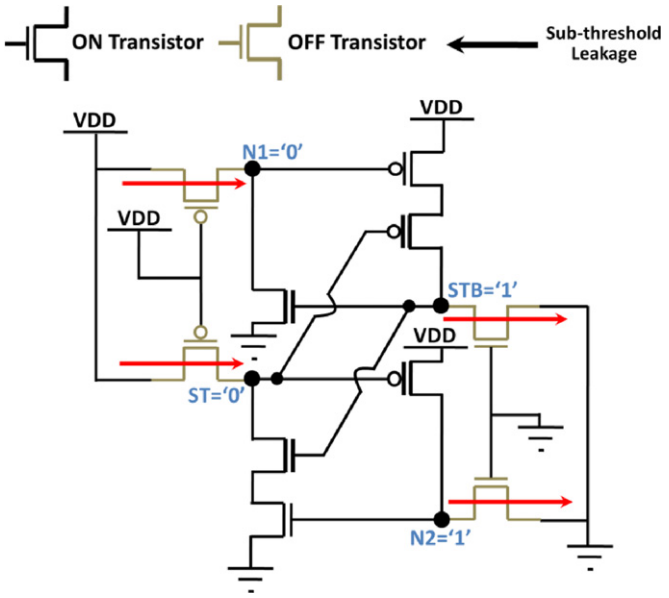

Fig. 2. Sub-threshold leakage current components in RCS SRAM cell when zero is stored in the cell.

- RCS SRAM cell releases the stored data on static read port (ST node or STB node in Fig. 1) and has no dynamic read port for reading the stored data in cell, when this cell is used as memory cell in array of memory cell in embedded cache memory.
- Cache-resident memory values of ordinary programs exhibit a strong bias towards zero [7,8]. Thus, most of bit values resident in the cache are zero. However, in RCS SRAM cell, when zero is stored in the cell, there are four sub-threshold leakage current components which they pass through one OFF transistor and these transistors have $|V_{DS}| = V_{DD}$, as shown in Fig. 2. Consequently, RCS SRAM cell consumes significant static power when zero is stored in this cell.
- Unsuccessful write operation due to random variations in process parameters. To investigate this issue, we consider the following scenario:
  - drivability of access transistors including M1, M2, M3 and M4 decreases (weaker access transistors) and drivability of driver transistors including M5, M6, M7, M8, M9 and M10 increases (stronger driver transistors) due to intra-die random variations or intra-die systematic variations (in intra-die random variations shifts in a parameter of two neighboring transistors are completely independent [3], and in intra-die systematic variations shifts in a parameter of one transistor depends on the shift of that parameter of a neighboring transistor [3]).