Microelectronics Journal 43 (2012) 838–847

Contents lists available at SciVerse ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

M-IVC: Applying multiple input vectors to co-optimize aging and leakage

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ARTICLE INFO

Article history:
Received 10 October 2011
Received in revised form
11 June 2012
Accepted 18 June 2012
Available online 17 July 2012

Keywords:
NBTI
Leakage
Co-optimization model
Multiple input vectors
Duty cycle

ABSTRACT

With technology scaling, aging effect and leakage pose significant challenge on the reliability of integrated circuits. Existing techniques on co-optimizing circuit aging and leakage either implement in an intrusive way or rely on input vector control (IVC) method. However, intrusive schemes increase the design complexity and induce extra delay and area overheads. IVC method becomes ineffective as the circuit scale increasing. In this paper, a non-intrusive scheme exploiting multiple input vectors (M-IVC) is proposed to co-optimize NBTI-induced degradation and leakage when the circuit steps into standby mode. M-IVC grounds on a new co-optimization model which formulates both the NBTI-induced delay degradation and the average standby leakage as the function of duty cycle. This co-optimization model facilitates to identify a set of optimal duty cycles which result in minimum NBTI-induced degradation and leakage simultaneously. To achieve the optimal duty cycles, an ATPG-like algorithm is proposed to generate multiple input vectors and determine the applying time for each vector. Experimental results demonstrate that with only a small number of vectors, M-IVC can effectively optimize NBTI-induced delay degradation and leakage together and keep the effectiveness as the time of standby period increasing.

1. Introduction

With aggressive scaling of the feature size, transistor aging poses significant challenge on the circuit reliability. Negative bias temperature instability (NBTI) is recognized as a paramount aging mechanism for nano-scale CMOS processes [1,2]. It rises the threshold voltage of PMOS with time and in turn increases the path delay gradually [3–6]. In the worst scenario, path delay can be increased up to 20% under long time NBTI effect (e.g., 10 year) [7,8]. On the other hand, leakage power increases as the supply/threshold voltage scaling and is recognized as another important design concern. In [9], Borkar predicted a 7.5 × increase in the leakage current and a 5 × increase in the total energy dissipation for every new microprocessor chip generation.

The current low power designs generally employ sleep or clock gating techniques to reduce the dynamic power. When the circuit steps into standby mode, the clocks will be gated to prevent unnecessary switching activities on the internal nodes in the circuit. The input signals of the gates thus remain unchanged persistently. However, such situation may cause large NBTI-induced delay degradation or leakage, or both of them simultaneously, because NBTI and leakage both strongly depend on the input pattern. Consequently, low power techniques like clock gating in some extent may exacerbate circuit aging and leakage, bringing significant impact on the circuit reliability.

Large amounts of research have been conducted for NBTI and leakage optimization. Some techniques were proposed to deal with NBTI-induced delay degradation, such as technology library mapping [10], body biasing [11] and aging-aware micro-architecture schemes [12–14], etc. However, these techniques did not consider the leakage optimization. On the other hand, the traditional leakage optimization methods, either in circuit level [15–17] or in micro-architecture level [18] did not take the aging optimization into account.

As for the co-optimization on NBTI and leakage, Chen et al. proposed to minimize leakage power by multi-V_{th} assignment in high-level synthesis considering service time requirement [19]. However, exploiting multi-V_{th} device will increase the manufacture cost considerably. Wang et al. proposed a gate replacement method in [20,21]. Such intrusive technique needs to change the original circuit design, thereby increasing the design complexity. Moreover, gate replacement also induces large area overhead (up to 13.26% in [20]) and about delay overhead of 5% [21].

Given that NBTI effect and leakage both strongly depend on the input pattern, some people exploited IVC method for NBTI and leakage co-optimization. In [5], Wang et al. explored the possibility that using the minimum leakage vector (MLV) to reduce NBTI-induced delay degradation. In the followed work

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http://dx.doi.org/10.1016/j.mejo.2012.06.007

Table 1
Dependency of NBTI effect and leakage on input pattern.

IV	NOR		NAND		IV	INV	
	D (%)	*L* (nA)	*D* (%)	*L* (nA)		*D* (%)	*L* (nA)
00	20	65.76	17	3.65	0	16.7	32.89
01	20	44.58	17	32.87	1	0	44.60
10	17.1	15.70	15.8	13.60			
11	0	0.59	0	89.16			

D, ratio of delay increase; *L*, leakage current; IV: input vector.

[22], they evaluated the effectiveness of IVC on simultaneously reducing circuit aging and leakage at different processes.

However, NBTI-induced degradation and leakage always manifest opposite dependency on the input pattern. Table 1 lists the delay degradation under 10-year NBTI effect and the leakage for some primitive gates with respect to different input vectors. Results in Table 1 are obtained from HSPICE simulation under PTM [24] 65 nm technology node. As shown in Table 1, obviously for NAND- and INV-gate, usually one input vector can lead to small leakage while causing large NBTI degradation, and vice versa. Therefore, only applying a single vector cannot achieve desirable result on NBTI and leakage co-optimization. In addition, one input vector has poor capability of controlling the signals on internal nodes in large-scale circuit. As the circuit scale increasing, IVC loses its effectiveness rapidly.

In this paper, we propose M-IVC, which exploits multiple input vectors to co-optimize NBTI-induced degradation and leakage when the circuit steps into standby mode. Our contributions include:

- A new co-optimization model is proposed which for the first time formulates both the NBTI-induced delay degradation and the average standby leakage as the function of duty cycle.
- An ATPG-like algorithm is proposed to generate multiple input vectors and determine the specific applying time for each vector. When the circuit steps into standby mode, these vectors will be applied in accordance with their applying times. Vector application in such non-uniform way can form the optimal duty cycles on the internal nodes in the circuit, thereby minimizing NBTI-induced degradation and leakage simultaneously.

The rest of the paper is organized as follows. Section 2 sketches out our scheme. Section 3 introduces the formulation of co-optimization model. Solving of the optimal duty cycles is presented in Section 4. Section 5 describes the ATPG-like algorithm and the hardware implementation. Experimental results are presented in Section 6 and finally, we conclude in Section 7.

2. Overview of M-IVC

M-IVC is realized in a way of reverse thinking, as shown in Fig. 1. First, a co-optimization model is established which formulates both the NBTI-induced delay degradation and the average standby leakage as the function of duty cycle. The nonlinear programming is then performed to identify a set of optimal duty cycles on the internal nodes in the circuit. Given the optimal duty cycles, an ATPG-like algorithm is proposed to generate multiple input vectors and determine the specific applying time for each vector.

M-IVC outperforms IVC for large-scale circuit. Multiple vectors can cover a portion of circuit nodes alternately, improving the control of signals on internal nodes. Moreover, applying multiple vectors can overcome the drawback in IVC that NBTI and leakage always show the opposite dependency on one vector.

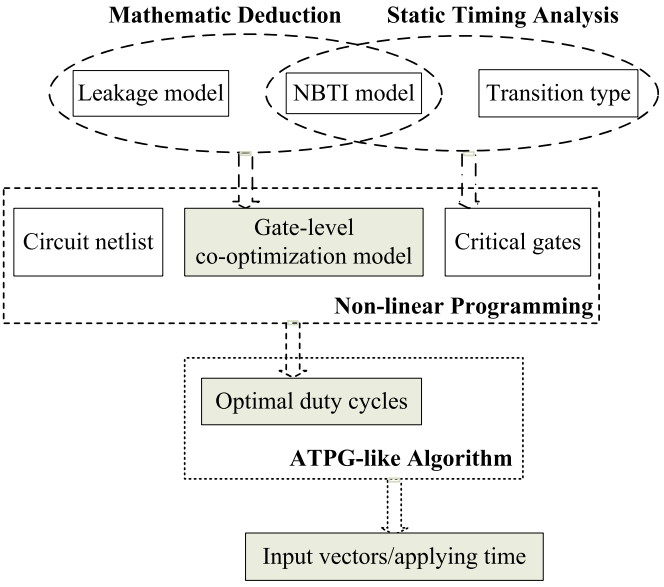

Fig. 1. Overview of M-IVC.

3. Formulation of co-optimization model

This section introduces the formulation of co-optimization model for NBTI and leakage. A large amount of the literature have showed that NBTI-induced delay degradation can be expressed as the function of duty cycle. In this paper, for the first time we proved that the average standby leakage in the whole circuit lifetime can also be formulated as the function of duty cycle based on the analysis of signal activity.

3.1. NBTI model

NBTI is a kind of aging mechanism which primarily affects PMOS device. Based on the long-term NBTI model [3], Wang et al. proposed a simplified model to predict the degradation on threshold voltage of the PMOS [8]

$$\Delta V_{th\_nbti} = b \cdot \alpha^n \cdot t^n \tag{1}$$

where $b = 3.9 \times 10^{-3} V\, s^{-1/6}$. α is the duty cycle, which denotes the percentage of time that the PMOS is in stress state (i.e., $V_{gs} = 0$). For diffusion species are H_2, n is around 0.16. t is the operational time that the circuit experienced. This simplified model has enough accuracy compared with the long-term one [8].

The duty cycle is the most important parameter in NBTI model because it reflects how long the PMOS is negative biased. The duty cycle is also equivalent to the statistical signal probability [8] (here, the signal probability is defined as the probability that the input signal is logic '0'). For example, assume that the signal probability *sp* on a gate input for a period of time *T* is 0.5. We can say that the PMOS connected to this gate input has been stressed for 0.5 *T* during the time *T*. Hence the duty cycle on this gate input is 0.5 correspondingly.

Based on the well-known alpha-power law [25], propagation delay of the gate can be approximately recognized as the linear function of threshold voltage. Therefore, combining with Eq. (1), the propagation delay from input node *i* of the gate to the gate