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Designing of low-power data oriented adders

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ABSTRACT

The paper presents an idea of designing of low-power adders addressed to specific data processing. Mainly, the idea consists in proper choosing of 1-bit full adder cells for given probability of summed data, to obtain reduction in consumed power. Additionally different structures of the cells can be used, in one design, if it leads to reduction of power dissipation. To proper choice of structures of 1-bit full adders theirs energy characteristic versus summed data is needed. So, at the beginning we present results of assessment of a few 1-bit adder cells selected from literature and designed in UMC180 CMOS technology. The extended model of power consumption, taking into consideration input vector changes, was used, giving more accurate values than traditional model based on switching activity only. Thanks to the use of this model, obtained results allow detailed analysis of 1-bit adders on account of the using them in designing of low-power multi-bit adders summing specific data. Based on the results of analyses and given characteristic of summed data, appropriate full adder cells can be chosen to the final design of low-power data oriented adder. In specific case, cells which are made in different techniques can be used in multi-bit adder. A few examples are shown at the end of the paper.

1. Introduction

A summation is one of fundamental operations performed in today computer systems. It is the most important in digital signal processing, which is related to all kinds of digital filtration and digital audio and video processing, ubiquitous in today mobile devices. Taking into account execution of a program by the processor, processing digital signal in real time, adding operation is about 72% of all executed instructions in a prototype DLX, RISC processor [1]. However, in popular and widely used processors with ARM core, adding operation is almost 80% of theirs execution time [2]. Therefore, multidimensional optimization of adders used in today processors design is very important. In this paper authors take into account four popular structures of 1-bit full adders in aspect of power consumption.

The idea of using extended model of power dissipation and results of 1-bit adder cells assessment for designing of low-power data oriented multi-bit adders was firstly mentioned in [3]. There are plenty of papers on design of low-power adders, both 1-bit full cells and multi-bit structures. Researchers use different algorithms for adding and various structures for multi-bit adders [4]. Some of them are very complex [5], and uses multi-dimensional optimization [6]. Usually authors do not consider non-uniform probability of signals changing for individual inputs and they use traditional model of power dissipation based on switching activity only and constant value of load capacitance. In [7] authors present results of power dissipation comparison of two the most widely used binary addition algorithms Weinberger and Ling implemented in Kogge–Stone structure of adder. Obtained results have shown that one algorithm is better than other in case of lower probability of input signals being one. And the situation changes in opposite case. However authors examined adders for various input signals probability but they assumed the same values of signal probability for all inputs. They used traditional activity of circuit – switching activity, which was calculated based on equations. Final conclusion is that selection of energy efficient addition algorithm is possible based on switching activity analysis. In our approach we propose to build adder with using different full adder cells, based on detailed analysis of theirs switching activity and using extended model of power dissipation. In [8] authors propose usage of different kind of full adder cells to build chain of adders. But their motivation is to use low-power cells, usually degrading output voltage swing, mixed with those which can improve logic signals.

Generally, in the paper, authors propose a method of selecting the best 1-bit cells, which allows building a multi-bit adder to processing of strictly specified data. The design procedure and examples are preceded by full adders' description and its energy parameters assessment. Section 2 describes adder cells and selection of example structures, which were designed and further their parameters were assessed. In Section 3 layouts of example adders, designed in UMC 180 nm CMOS technology, are shown. Next, extended power consumption modeling and results of appropriate assessment of energy parameters are presented. Section 4 contains

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analysis of usage previously designed cells for low-power multi-bit adders designing. Next, some examples are shown and the paper is concluded in Section 5.

2. Selection of full adder cells

Adder it is arithmetic circuit, which adds two N-bit numbers. The result is N-bit number and one bit of carry. Additionally carry input can be taken into consideration. The basic circuit, which allows building adders of any size, is 1-bit full adder. There are several strategies for basic cells connection to build larger adders. The sum (s_i) and carry (c_{i+1}) outputs of 1-bit full adder, summing a_i, b_i, and c_i (carry input), can be described by following equations:

$$s_i = c_i \oplus a_i \oplus b_i \tag{1}$$

$$c_{i+1} = a_i b_i + a_i c_i + b_i c_i \tag{2}$$

It can be directly implemented in CMOS technology after using of de'Morgan laws. But another implementation can be found if (1) or (2) will be transforming.

There are many realizations of 1-bit full adders can be found in literature. But unfortunately the ones with the smallest number of used transistor do not have good performance parameters. Especially they have not full swing output signal when designed in standard CMOS technology [9,10]. Moreover searching of new low-power adders are not the main purpose of the paper. So, for example, only four structures have been chosen and designed in CMOS UMC 180 nm technology for further analysis and usage in multi-bit adders design. The structures are described below.

2.1. Standard CMOS adder

First designed structure of 1-bit full adder is conventional CMOS circuit consists of 28 transistors [11]. Transforming (1) to the following formula:

$$s_i = \overline{c_{i+1}}(a_i + b_i + c_i) + a_i b_i c_i \tag{3}$$

and using complex gates, with appropriate transistors reducing, the schematic diagram of the T28 full adder is shown in Fig. 1.

Twelve of transistors are used to produce carry output function, and remaining sixteen ones for sum output. Additionally, delay of carry output is added to delay of sum, which is delay of whole circuit. Relatively large number of transistors beside complexity of theirs interconnections can cause high power consumption. But from other hand it is fully complementary circuit. It has high robustness and can its operation is independent of supply voltage.

2.2. Transmission gate adder

The adder is built using a set of appropriate connected transmission gates in such a way that input signal is transmitted to the output in order to implement of summation operation. It can be perceived as extended pass transistor logic technique. Full transmission gates require complementary signals for theirs control and additional inverters are added to the circuit. In consequence TGA considered in this paper consists of 12 transistors in transmission gates and remaining of total 20, are used in inverters [11]. Fig. 2 shows schematic diagram of the adder.

Usage of full transmission gates instead of single transistors ensures full voltage swing at the circuit outputs. This adder has lower number of transistors than previous, but from other hand there are no isolations between inputs and outputs.

2.3. Bridge style adder

In bridge design style of circuits an additional transistor is used and it is called bridge. The transistors create a conditional conjunction between two circuit nodes. And in consequence new path from supply to the output can be formed [12]. If the full adder is described by functions represented in sums of product as follows:

$$s_i = a_i b_i c_i + a_i \overline{b_i}\,\overline{c_i} + \overline{a_i} b_i \overline{c_i} + \overline{a_i}\,\overline{b_i} c_i$$
$$c_{i+1} = a_i b_i c_i + a_i b_i \overline{c_i} + \overline{a_i} b_i c_i + a_i \overline{b_i} c_i \tag{4}$$

Then it can be implemented with bridge design style, as shown in Fig. 3. Frames in the figure mark bridge transistors.

That implementation requires using of 26 transistors for sum and carry function. But each input has to be negated, so three inverters are needed. The total number of transistors is 32. It is

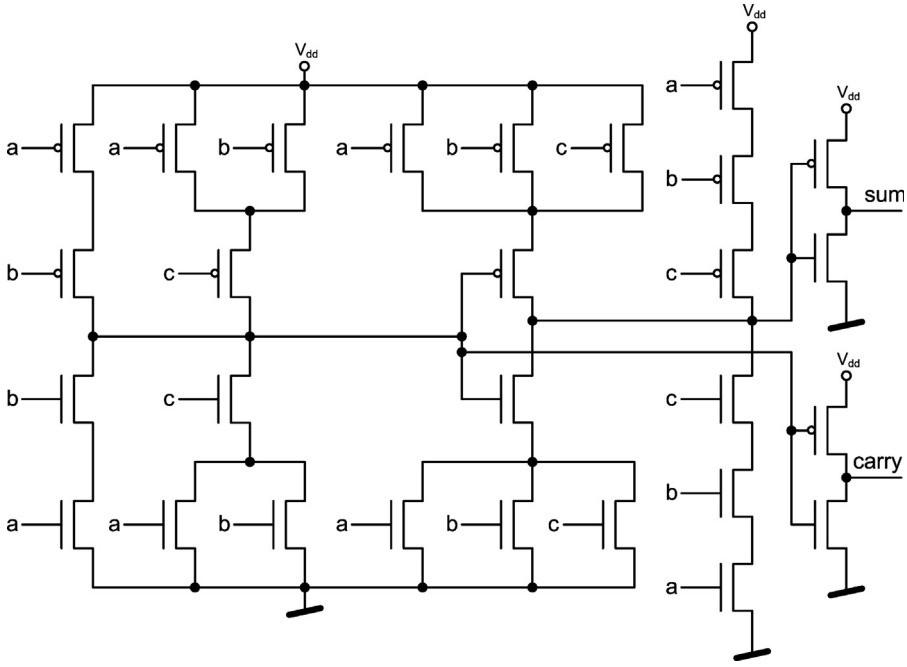

Fig. 1. The standard 28-transistor CMOS full adder.