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ScienceDirect
Microelectronic Engineering 85 (2008) 89–92
MICROELECTRONIC ENGINEERING
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High breakdown voltage 4H-SiC MESFETs with floating metal strips

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Received 22 December 2006; received in revised form 6 March 2007; accepted 3 April 2007
Available online 22 April 2007

Abstract

A high breakdown voltage 4H-SiC MESFET with floating metal strips (FMS) was proposed. The maximum electrical field of the MESFET gate is clamped after surface depletion layer punch through to FMS. The optimized results showed that the breakdown voltage of the 4H-SiC MESFET with two strips and one strip are 180% and 95% larger than that of the conventional one without FMS and meanwhile maintain almost same saturation drain current. The maximum theoretical output power density of the 4H-SiC MESFET with two strips and one strip are 14.5 W and 10.0 W compared to 4.8 W of the conventional structure. The cut-off frequency (f_T) of 14.7 GHz and 15.6 GHz and the maximum oscillation frequency (f_{max}) of 44.8 GHz and 48.7 GHz for the 4H-SiC MESFET with two strips and one strip are obtained respectively, which is just a little bit lower than that of the conventional structure.

Keywords: Breakdown voltage; 4H-SiC; MESFET; Floating metal strip

1. Introduction

Silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) is a promising candidate for high power radio frequency (RF) application even under extremely worse conditions because of its excellent thermal and electrical properties [1,2]. With the recent progress in SiC epitaxial material and device process, impressive performances for SiC MESFETs has been reported [3,4]. Although the experimental and simulation results in previous work showed that SiC MESFETs have superior breakdown characteristics compared to those made with Si and GaAs, it is still worth investigating potential ways to increase the breakdown voltage to better meet the increasing demand for high power applications. Many researches on SiC MESFETs showed that its breakdown happened at the gate corner nearer to the drain side on the device surface due to the electric field crowding [5,6]. In order to suppress the peak electric field as well as alleviate the electric field crowding in the drain side gate corner, recently, field plate (FP) SiC MESFETs was simulated and fabricated to obtain a high breakdown voltage [7,8]. However, with the employing of FP, device fabrication process and parameter optimization become complex due to appearance of additional dielectric layer. In this paper, utilizing similar working principle with floating metal rings (FMR) which is an effective edge termination (ET) structure widely used in planar Schottky barrier diodes (SBDs), 4H-SiC MESFETs with floating metal strips (FMS) were investigated to allow a high breakdown voltage for the first time. This work is a continued research to investigate the effectiveness of floating metal on planar 4H-SiC device based on our pervious work for MMIC SBDs [9]. In comparison with complex fabrication process of FP structure, FMS can be fabricated easily using same process with the MESFET gate.

2. Device structure

Fig. 1a shows the schematic cross-section view of the proposed 4H-SiC MESFET with FMS. The device structure is stacked by a semi-insulating substrate, a p-type buffer layer, an n-type channel layer and a highly doped n-type cap layer. Other than the normal gate, there still have metal

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doi:10.1016/j.mee.2007.04.121

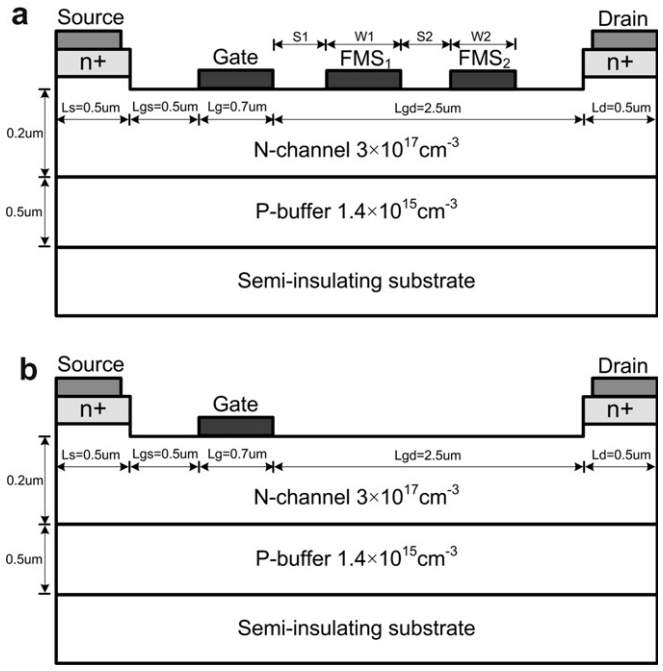

Fig. 1. Schematic cross-section view of 4H-SiC MESFETs (a) proposed structure with FMS and (b) conventional structure without FMS.

strips in the device surface. The device parameters are as followed: source length $L_s = 0.5$ μm, gate-source spacing $L_{gs} = 0.5$ μm, gate length $L_g = 0.7$ μm, gate-drain spacing $L_{gd} = 2.5$ μm and drain length $L_d = 0.5$ μm. $W1$ and $W2$ are width of the first and second metal strip, respectively. $S1$ is spacing between the normal gate and the first metal strip and $S2$ is spacing between the first and second metal strip. $W1$, $W2$, $S1$ and $S2$ will be optimized in the following section. The doping concentration of n-cap layer is 2×10^{19} cm^{-3}. The channel thickness is 0.2 μm and doping concentration is 3×10^{17} cm^{-3}. The doping and thickness of the P-buffer layer are 1.4×10^{15} cm^{-3} and 0.5 μm, respectively. The substrate is semi-insulating substrate. Nickel was chosen for the gate and FMS Schottky contact with a work function of 5.1 eV. In order to have a meaningful comparison, the conventional structure has same device parameters with the proposed structure, shown in Fig. 1b, was simulated. The devices were simulated using 3-D simulation tool ISE [10] with 4H-SiC material parameters. FMS was conducted by a zero external current boundary condition [11].

3. Results and discussion

According to FMR theory, the spacing between the normal gate and the first strip as well as the spacing between any two neighboring strips are crucial to improve the breakdown voltage (V_b) of the 4H-SiC MESFETs. Apart from it, the breakdown voltage is also influenced by strip's width. Therefore, the device parameters of $S1$, $W1$, $S2$ and $W2$ were optimized and fixed at the beginning. Fig. 2 shows the contour of the calculated V_b with $S1$ and $W1$ as parameters for 4H-SiC MESFETs with one FMS. The simulation result reveals that the highest breakdown voltage of the 4H-SiC MESFET with one strip can be obtained within a certain range. In order to keep chip area as small as possible, $S1 = W1 = 0.5$ μm is selected. Considering the screen effect of the first strip from the influence of the second strip on the normal gate, $S1$ and $W1$ were fixed at 0.5 μm when two strips were employed. Fig. 3 shows the contour of the calculated V_b with $S2$ and $W2$ as parameters for 4H-SiC MESFETs with two FMS. $S2 = 0.5$ μm and $W2 = 0.4$ μm were fixed to obtain the largest breakdown voltage as well as to keep smaller chip area. It can be seen from the above two contours that the V_b of 4H-SiC MESFETs is improved greatly after employing FMS structure. Even so, the exact location of the strips is critical to its effectiveness in increasing the V_b of 4H-SiC MESFETs. In the following discussion, $S1 = W1 = 0.5$ μm, $S2 = 0.5$ μm and $W2 = 0.4$ μm were used.

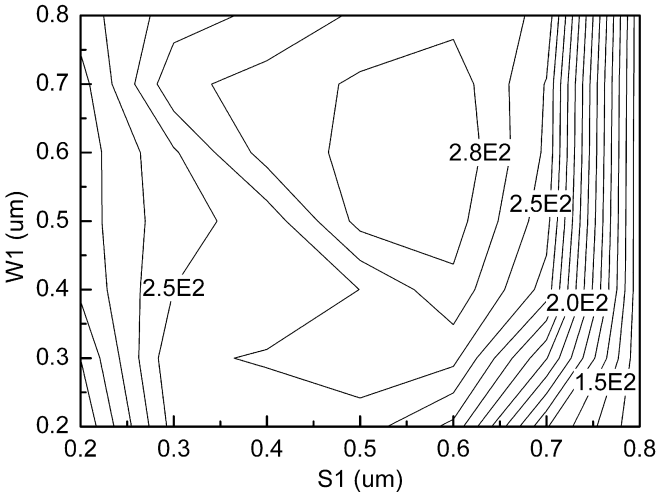

Fig. 2. Contour of the calculated V_b with $S1$ and $W1$ as parameters for 4H-SiC MESFETs with one FMS.

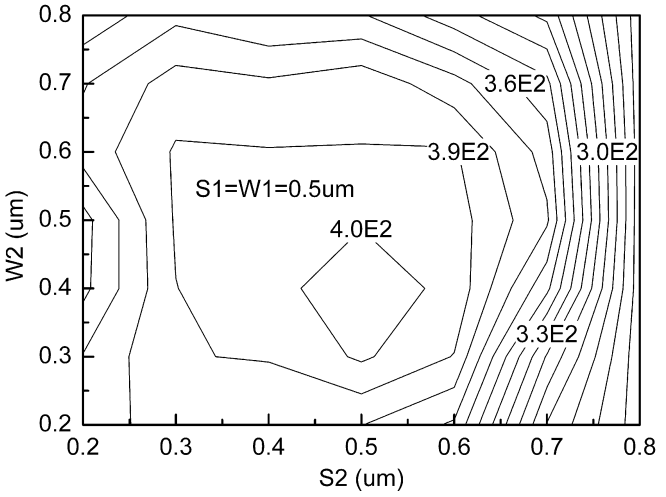

Fig. 3. Contour of the calculated V_b with $S2$ and $W2$ as parameters for 4H-SiC MESFETs with two FMSs.