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# Conduction mechanisms in $Ta_2O_5$ stack in response to rapid thermal annealing

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**Abstract**

The influence of the rapid thermal annealing (RTA) in vacuum at 1000 °C on the leakage current characteristics and conduction mechanisms in thermal $Ta_2O_5$ (7–40 nm) on Si has been studied. It was established that the effect of RTA depends on both the initial parameters of the films (defined by the oxidation temperature and film thickness) and annealing time (15–60 s). The RTA tends to change the distribution and the density of the traps in stack, and this reflects on the dielectric and leakage properties. The thinner the film and the poorer the oxidation, the more susceptible the layer to heating. The short (15 s) annealing is effective in improving the leakage characteristics of poorly oxidized samples. The RTA effect, however, is rather deleterious than beneficial, for the thinner layers with good oxygen stoichiometry. RTA modifies the conduction mechanism of $Ta_2O_5$ films only in the high-field region. The annealing time has strong impact on the appearance of a certain type of reactions upon annealing resulting to variation of the ratio between donors and traps into $Ta_2O_5$, causing different degree of compensation, and consequently to domination of one of the two mechanisms at high fields (Schottky emission or Poole–Frenkel effect). Trends associated with simultaneous action of annealing and generation of traps during RTA processing, and respectively the domination of one of them, are discussed.
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*Keywords:* High-*k* stack; Tantalum pentoxide; RTA; Conduction mechanisms

## 1. Introduction

A number of materials with high dielectric constant (high-*k*) are currently under consideration to replace $SiO_2$-based insulators as a key component of high density dynamic random access memories (DRAMs). Among high-*k* oxides, $Ta_2O_5$ is a candidate of choice in terms of desired level of stored charge for Giga scale DRAMs [1–5]. In order to improve the electrical characteristics, the $Ta_2O_5$–Si system systematically requires post-fabrication treatments at relatively high temperature. The annealing processes usually favor the growth of unavoidable interfacial layer with lower-*k* which is related to the thermodynamical instability of the high-*k* insulators in direct contact with Si against formation of $SiO_2$. The interfacial layer reduces the global dielectric constant of the stack but at the same time ensures better interfacial properties. The lower-*k* layer in series with $Ta_2O_5$ can in some cases even nullify the benefit of $Ta_2O_5$ as a high-*k* material with a capacitance corresponding to the desirable value of equivalent oxide thickness. Another problem comes from crystallization effects appearing usually at temperatures above about 600 °C [6–10]. Although crystalline $Ta_2O_5$ has a higher dielectric constant than amorphous one its leakage current can be higher (the grain boundaries could serve as an additional leakage path). The crystallization is unacceptable for high density devices because it leads to poor point-to-point uniformity and variation of the parameters from one device to another. On the other hand, it is generally recognized that the annealing repairs the oxygen vacancies and various structural non-perfections in the initial $Ta_2O_5$ films; thus the leakage current could be effectively reduced [7,11–13]. Hereby although post-fabrication long

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time annealing at high temperatures can in some cases effectively reduce the leakage current (stimulating net annealing) one has to consider other effects which might influence the physical and electrical properties of the films. Rapid thermal annealing (RTA) processes are suggested as an alternative solution of this annealing problem of high-$k$ dielectrics, and in particular of $Ta_2O_5$ [14–16]. Due to the reduced thermal budget it is expected RTA to overcome some negative effects of long-term annealing processes. Very short annealing times, good control of the temperature and process simplicity are among the advantages of RTA. Efforts have been made to establish the influence of RTA in various ambients on the parameters of thin $Ta_2O_5$ films. As a whole, however, the RTA process-$Ta_2O_5$ properties correlation is not known precisely. Previously [17], we have reported that RTA in vacuum affects electrical and physical parameters of thermal $Ta_2O_5$ on Si, and the effect strongly depends on the initial properties of the films. It was found that the low quality thin films (i.e. obtained at 400 and 500 °C) could benefit from this type of treatment mainly in terms of leakage currents. The investigation here is focused on the relationship between the mechanisms of conductivity in (7–40 nm) $Ta_2O_5$ on Si and the fabrication conditions, namely oxidation temperature and parameters of rapid thermal annealing.

## 2. Samples and experimental set-up

The test samples were obtained by deposition of Ta films (rf sputtering of Ta target in argon ambient) on cleaned p-type 15 Ω cm (1 0 0) Si wafers with a subsequent oxidation in dry $O_2$. Four oxidation temperatures $T_{ox}$ (400, 500, 550 and 600 °C) were used, low enough to prevent formation of tantalum silicides and also to avoid or at least to minimize the formation of interfacial layer between $Ta_2O_5$ and Si substrate. After oxidation the samples were subjected to rapid thermal annealing in vacuum ($5 \times 10^{-5}$ Torr) at a temperature of 1000 °C, for annealing times $t_a = 15$, 30, and 60 s. Details on both the oxidation process and RTA treatment can be found elsewhere [17–19]. The thickness $d$ of the films is in the range 7–40 nm ($d$ and the refractive index $n$ were determined ellipsometrically, $\lambda = 632.8$ nm; $d$ is the total thickness of the films including the interfacial layer). Electrical measurements were performed on MOS capacitors with Al gate, (gate area of $1.96 \times 10^{-3}$ cm$^2$). Al was evaporated by resistive heating. The capacitance voltage ($C$–$V$) and current voltage ($I$–$V$) characteristics were analyzed before and after RTA step. The oxide charge $Q_f$ was evaluated from hf (1 MHz) $C$–$V$ curves. The dielectric constant of the layers $\varepsilon_{eff}$ was determined from the capacitance value $C_0$ in accumulation using the ellipsometrically measured thickness. Since the main purpose was to study the impact of RTA process on the conduction mechanisms in $Ta_2O_5$, the $I$–$V$ measurements were carried out only at negative gate voltages (Si substrate is kept in accumulation; the electric field is applied across the dielectric and the forward curve is the main characteristic of the stack). Ramped $I$–$V$ curves with a ramp rate of 0.1 V/s were used to investigate the leakage current at low and high voltages. The experimental $I$–$V$ data were plotted to get the normalized current density vs. electric field curve. All electrical measurements were performed at room temperature.

## 3. Results and discussion

### 3.1. Dielectric properties and C–V curves

The values of the refractive index $n_t$ of the bulk $Ta_2O_5$ were estimated from the thickness dependence of measured refractive index in an assumption of a double layer nature of $Ta_2O_5$/Si structures (the stack consists of bulk $Ta_2O_5$ and an interface layer at Si) [18]. Under this consideration $n_t$ was found to be 2.24 for $T_{ox} = 400$ and 500 °C, and 2.25 for the higher temperatures. RTA does not affect $n$ for all $t_a$, suggesting that the films density remains the same as before the annealing. ($n = 1.6$ for $d = 7$ nm; $n = 2.1$ for $d = 15$ nm; and $n = 2.15$ for $d = 40$ nm) Representative data for the effect of $t_a$ on $\varepsilon_{eff}$ are shown in Fig. 1 (the data for the films obtained at $T_{ox} = 550$ and 600 °C are nearly the same). The as-grown 400 °C layers were too leaky to obtain proper $C$–$V$ curves, which prevented the determination of $\varepsilon_{eff}$. After annealing their dielectric constants were close to those for the films obtained at higher temperatures, and remain annealing time independent. The values of $\varepsilon_{eff}$ were about 5 for the 7 and 15 nm as-grown films and ~9 for the 40 nm ones independently of $T_{ox}$. Generally, the increase of $\varepsilon_{eff}$ with d means an increase of the density for the thicker films. The thickness dependence reflects also the influence of the interfacial layer at Si on the stack capacitance. According to the previous XPS analysis [20], this layer is actually $SiO_2$-like with a small amount of $Si_2O$. The thickness of the interfacial layer for the technological conditions used here is 1.8 nm as determined by transmission electron microscopy (TEM) [8], and during

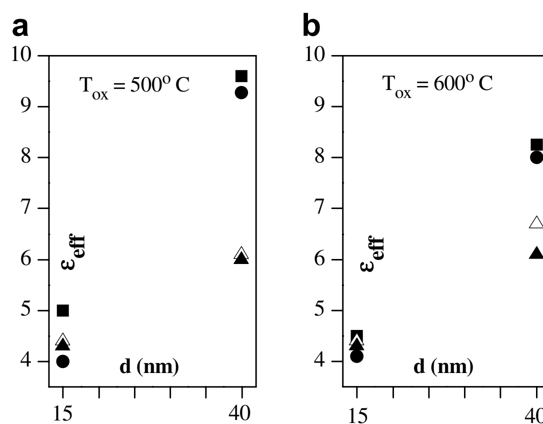


Fig. 1. Values of the effective dielectric constant for 15 and 40 nm $Ta_2O_5$ before ■ and after RTA: ● – $t_a = 15$ s; Δ – 30 s; ▲ – 60 s. (a) $T_{ox} = 500$ °C and (b) $T_{ox} = 550$ and 600 °C.

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