Microelectronics Journal 45 (2014) 375–381

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Frequency presetting and phase error detection technique for fast-locking phase-locked loop

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ARTICLE INFO

Article history:
Received 13 October 2012
Received in revised form
2 August 2013
Accepted 7 January 2014
Available online 15 March 2014

Keywords:
Fast-lock
Frequency tracking
Phase error detector
Phase-locked loop

ABSTRACT

A frequency presetting and phase error detection technique for a fast-locking phase-locked loop (PLL) is presented. The frequency difference between the reference clock and the divided VCO output clock is detected by the frequency presetting circuit. The frequency-presetting scheme allows the control voltage to be brought close to the target voltage with small initial frequency error. The phase error detector further reduced the locking speed by increasing the bandwidth of PLL through altering the supply current in the charge pump according to the phase error between the reference clock and the divided VCO output clock. The settling time of PLL can be significantly reduced afterwards. The settling time is reduced by 86%. The proposed PLL has been implemented in a 0.35 μm CMOS process, with a supply voltage of 3.3 V.

1. Introduction

The phase-locked loop (PLL) architecture is widely used in clock generators in high performance microprocessors and high-speed digital communication systems. The optimization of PLL performance has some limitations. To have the optimal jitter performance for a specified PLL, the loop bandwidth should be carefully chosen according to the requirements of the applications. In the telecommunications system, such as in the switch between the communication channels, a fast response of PLL is required, particularly for frequency synthesis applications. Fast PLL can also help in reducing the power-up latency of the system and in saving energy for longer battery life in mobile products. To reduce the settling time, a wide loop bandwidth of a PLL would be needed. However, with wide bandwidth, the output phase jitter increases due to external noise. There is a trade-off between the phase jitter and settling time [1–5].

In this work, a frequency-to-voltage converter (FVC) is used to speed up the frequency acquisition time of the PLL [5]. The reference clock and divided voltage-controlled oscillator (VCO) clock is converted to voltage by FVC. The voltage difference is able to force the control voltage of the VCO to have a frequency close to the reference clock. However, because the phase error still occurs between the reference clock and the divided VCO clock, the phase error detector is able to afford a wider loop bandwidth for quick reduction of the phase error. The combination of both processes leads to a short locking time. The proposed PLL also avoids the trade-off between phase jitter and settling time. This paper is organized as follows. In Section 2, the architecture of the proposed circuit is introduced. Section 3 presents the circuit realization of the proposed PLL, which incorporates the fast-locking technique. Section 4 shows the measurement results. Finally, Section 5 concludes this paper.

2. Architecture of the proposed circuit

A linear model representing the charge pump PLL in the locked state is presented in Fig. 1. The closed-loop transfer function with a first-order low-pass filter can be expressed as

$$H(s)=\frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)}=M\frac{2\varsigma(s/\omega_n)+1}{(s/\omega_n)^2+2\varsigma(s/\omega_n)+1} \tag{1}$$

This equation is in a standard form of a first-order low-pass system with the damping factor (ζ) and natural frequency (ω_n) defined as follows:

$$\varsigma=\frac{R_S}{2}\sqrt{\frac{I_P K_{\text{VCO}} C_S}{M}} \tag{2}$$

$$\omega_n=\sqrt{\frac{I_P K_{\text{VCO}}}{MC_S}} \tag{3}$$

where I_P is the charge pump current, K_{VCO} is the gain of VCO, and M is the divider ratio.

From Eq. (3), the natural frequency is proportional to the I_P. Therefore, by increasing I_P, the natural frequency is also increased

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http://dx.doi.org/10.1016/j.mejo.2014.01.003
0026-2692

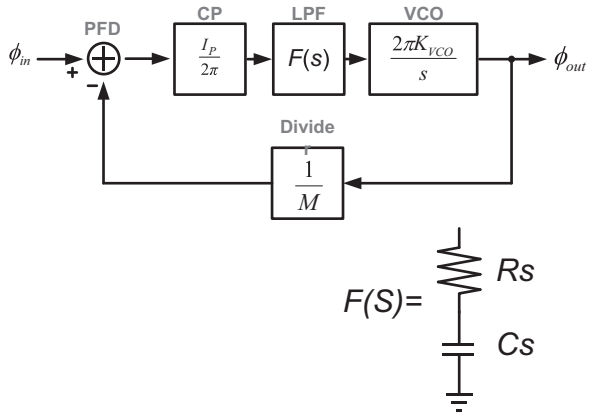

Fig. 1. Linear mode for PLL.

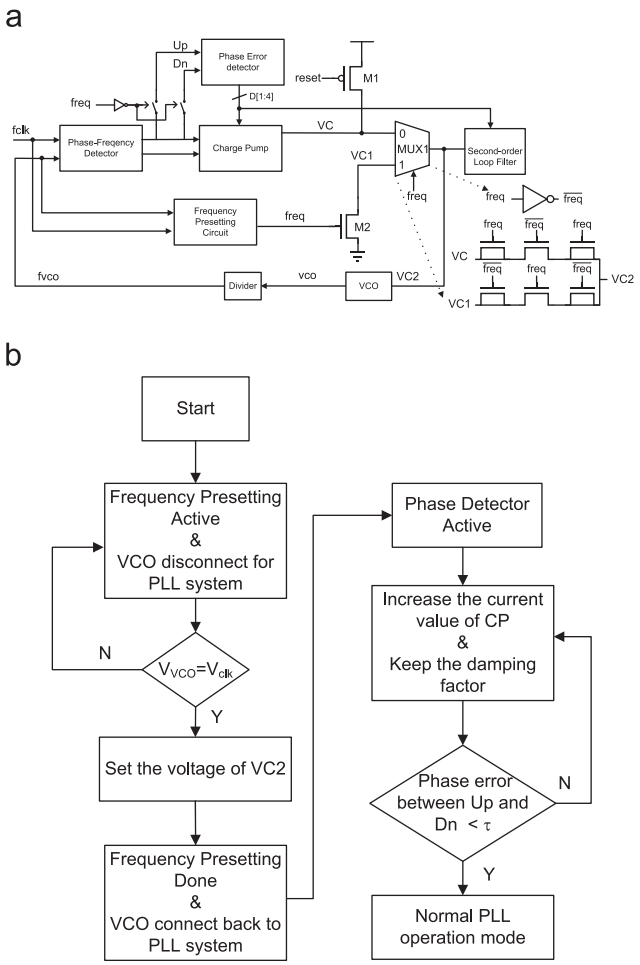

Fig. 2. (a) Proposed fast-locking PLL. (b) The flowchart of the proposed PLL.

but ζ needs to remain constant. The lock time is inversely proportional to the natural frequency. Therefore, the lock time is reduced by increasing the supply current of charge pump (I_P).

The block diagram of a frequency presetting and phase error detection technique for fast-locking phase-locked loop consists of a frequency presetting circuit, a phase error detector, a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump (CP), a second-order loop filter, multiplexer (MUX1) and divider, as shown in Fig. 2(a). The acquisition process of the proposed PLL can be divided into two parts: frequency tracking and phase error reduction. Before the PLL starts, the external signal "reset" charges the control voltage VC to VDD by transistor M1. At the beginning, the VC is connected to control voltage two (VC2), as the signal "freq" is low. The oscillation frequency of the VCO is controlled by the VC2 and has the highest frequency at the initial condition. When the proposed PLL starts up, it first works in frequency tracking. The frequency tracking is performed by the frequency presetting circuit. The frequency presetting circuit determines the frequency difference between fclk and fvco. If there is a frequency difference between them, the signal "freq" goes high and turns on transistor M2. M2 pulls down the control voltage one (VC1). At this point, VC1 and VC2 are connected. The oscillation frequency of the VCO will move toward the frequency of reference clock (fclk) by disconnecting the VCO from the charge pump by MUX1, as shown in Fig. 2(a). The frequency tracking is terminated, as the fclk and fvco reach almost the same frequency. Afterward, the "freq" signal goes low. The node of VC2 is connected to the node of VC. The frequency of the VCO is controlled by the CP, PFD and phase error detector. The PLL system enters the phase error reduction stage. The Up and Dn pulses are generated by the PFD, which is able to turn on the phase error detector, as the "freq" signal is low. The phase error detector quantizes the phase difference between the Up and Dn pulses. The phase difference is converted into 4-bit digital code, D[1:4], to increase the supply current of the charge pump. According to Eq. (3), the loop bandwidth is wider due to the increased supply current of the charge pump. The 4-bit digital code, D[1:4], also changes the resistance of the resistor in the second-order loop filter to keep the damping factor constant. The loop bandwidth is adaptive to change with D[1:4] to achieve quick compensation of the phase error. Finally, once the loop approaches the locked state, the phase error is adequately small. The phase error detector will be turned off by itself. The loop bandwidth then returns to the initial designed value (small bandwidth). The PLL returns to normal operation. Therefore, the proposed PLL can settle down in a very short time compared to conventional PLL.

Fig. 2(b) illustrates the flowchart of the proposed PLL. From the startup, the frequency setting is active. This is achieved by converting the frequency of fvco and fclk into voltage Vvco and Vclk, respectively. When the voltage of Vvco has the same voltage as Vclk, the voltage of VC2 is set to a desired value. The frequency setting circuit is active at only one time to set the voltage of VC2. Afterward, the VCO will reconnect to the PLL system, and the phase error detector becomes active. The phase error detector quantizes the phase difference between Up and Dn. The phase error between Up and Dn is proportional to the phase difference between fclk and fvco. The smallest quantization step is τ. The current in the charge pump is increased when the phase difference is greater than τ. The damping factor of the system is kept constant by reducing the resistance in the loop filter. When the phase error is smaller than τ, the PLL lock-in procedure is reset to normal mode. The PFD continuously decreases the phase error until the locked state.

3. Circuit implementation

3.1. Frequency presetting circuit

Fig. 3 shows the block diagram of the frequency presetting circuit, which consists of two frequency-to-voltage converters (FVC) [5], two D-type flip-flops (DFFs), an inverter and a comparator (Comp). The frequency of fvco and fclk are transferred into voltage levels (Vvco and Vclk) by the FVC. The output of the frequency presetting circuit, "freq", is low at the beginning. After the reset of PLL, the frequency of the fvco is higher than the frequency of the fclk because the voltage of VC2 is higher as the