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Efficient nonrectangular shaped voltage island aware floorplanning with nonrandomized searching engine

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ABSTRACT

Multi-supply voltage (MSV) technique is one of the efficient ways to reduce power consumption. However, MSV makes the physical design much more complicated. Especially, the randomized algorithm consumes much time as the size of the problem increases and the constraint of rectangular shaped voltage island limits better solutions in terms of power. In this paper, a nonrectangular shaped voltage island (NSVI) aware floorplanning is proposed with nonrandomized searching engine for efficient floorplanning. With a generalized slicing tree, a hypergraph is generated according to the cores' legal voltage levels, which is favorable to cluster cores working under the same voltage level together so that the called NSVIs can be generated easily. The proposed approach can deal with the fixed-outline floorplanning and perform well under different aspect ratios. Experimental results on GSRC benchmark suites indicate that the proposed method can obtain better solutions with less CPU time than published methods.

1. Introduction

With the advance of transistor feature size and the development of system-on-chips (SoCs) technology, hundreds of intellectual property (IP) cores can be incorporated into one single chip. As a result, power density that causes thermal and reliability problems is one of the most important issues in SoC design. Since dynamic power is proportional to the square of the supply voltage, reducing the supply voltage is one of the most efficient ways. Therefore, multi-supply voltage (MSV) technology is presented and established with applying high voltage to critical cores and low voltage to noncritical cores without performance degradation for SoC design [1,2].

However, MSV technology may cause the overhead of power routings. To reduce the overhead, cores are clustered to voltage islands (VIs) according to their supply voltages and physical locations, and all cores inside one island operate at the same voltage level [3–5]. Nevertheless, a big challenge lies in handling the complexity inherent from effective power management of MSVs during physical design. Hence, physical design becomes more complicated than ever since island partitioning, voltage assignment, and floorplanning have to be optimized simultaneously under the constraints of area, power and timing [2]. Besides, further physical constraints such as fixed-outline [6–10], pre-placed cores [11], power/ground (P/G) network [12,13], temperature [14,15] make the problem even more complex. Moreover, level shifters are essential modules which convert signals among different voltage domains [16,17].

MSVs can be applied at floorplanning and placement stages [2,18–21] or post-floorplanning and post-placement stages [3,4,22–24]. Postprocessing is deemed to be an economic way to accomplish MSV design. However, since the floorplanning is fixed at this stage, the solution improvement of MSV design may be modest. In contrast, if the MSV was applied during floorplanning, the resulted solution quality could be improved significantly.

In [18], VI partitioning, voltage level assignment and physical level floorplanning are considered simultaneously. A graph is used to represent a partition solution of voltage islands, and then the solution is perturbed by simulated annealing (SA) algorithm in both chip-level and island-level until the final solution is obtained. In [19], thermal problem aimed at temperature reduction and hot spot elimination is studied. Genetic algorithm (GA) is used firstly to partition VIs and SA as a floorplanning searching engine is adopted. In [25], a voltage assignment technique based on dynamic programming is proposed. The optimal solution for the voltage assignment is found and level shifters are inserted between cores operating at different voltage levels. Finally, the power-network aware floorplanning is performed. In [2], an optimal floorplanning solution with VIs is proposed. Firstly, a normalized polish tree (NPE) [26] is employed to represent a floorplan candidate. Then, optimal VIs are obtained by dynamic

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programming for each candidate. At last, the floorplan candidates are perturbed by the SA searching engine and the optimal solution is found. All of the above mentioned works employ randomized algorithms such as GA and SA to search the solution space. However, the MSV design is a multi-objective optimization problem, which is not only hard to obtain an optimal solution in a reasonable time, but also difficult to find an optimized solution as the number of cores increases.

To facilitate the power routing, VIs in rectangular shapes are generated by a slicing tree structure [2,3]. However, this constraint on island shape may significantly degrade the solution quality [4,27]. By relaxing the rectangular shaped voltage island (RSVI) constraint, much better power savings can be achieved [27]. VI shape may trade off extra power network resource and cause large IR drop [4]. Therefore, apart from power, wirelength and white space, island shape has to be considered simultaneously for MSV based SoC design.

In the early floorplanning step, cores still have large flexibilities in shape and dimension. The floorplanning of nonrectangular cores such as L-shaped or T-shaped cores are widely explored in order to improve the packing quality [28,29]. Inspired from this, if the shape of VIs was extended to nonrectangular shapes, the power consumption might be reduced with less additional power network resource tradeoff. Hence, nonrectangular shaped voltage island (NSVI) can be formed by abutting several RSVIs, such as the L-shaped core (module) can be formed by two rectangular shaped cores. Different VI shapes might have different power consumption. Fig. 1 shows three possible types of VIs, where *a* is an irregular shaped island, *b* is an RSVI while *c* is a NSVI. Although the power from an irregular shaped island may consume less power than that from the corresponding RSVI, the irregular shape certainly is hard for the power routing since power ring is realized by the contour of the VI [30]. Generally, the RSVI has good shape and less power network resource, but may deteriorate the results in power consumption. In contrast, the NSVI is a compromised solution which may reduce the power consumption with less power network resource overhead.

Randomized algorithm, such as SA, is a classic optimization method for floorplanning. Starting from an initial floorplan, the solution quality is iteratively improved by perturbation and the algorithm is terminated until some pre-defined conditions are met. Randomized algorithm always consumes much time and does not scale nicely with the size of the problems. To speed up the CPU time, we adopt the nonrandomized searching engine for problem solving.

In this paper, an efficient VI aware floorplanning method is proposed for power reduction and CPU time improvement. For power reduction, the NSVI instead of RSVI is generated by relaxing the rectangular island shape constraint. To improve the CPU time, the nonrandomized searching engine is adopted. Our contributions can be summarized as follows:

(1) An MSV aware floorplanning method without randomized searching engine is proposed.

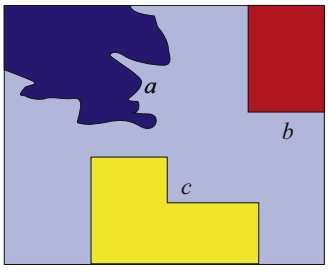

Fig. 1. The different island shapes in floorplan.

(2) A method to generate nonrectangular shaped VIs is presented.
(3) A hypergraph generation method is proposed to guide tree partitioning based on the cores' legal voltage levels.

The remainder of this paper is organized as follows. Preliminaries in Section 2 are described. The main approach including algorithm flow, details of hypergraph partitioning, NSVI generation and parameter setting are demonstrated in Section 3. The experimental comparison is shown in Section 4. Finally, a summary of the research findings is concluded.

2. Preliminaries

In this section, the problem is formulated and then the brief review of the generalized slicing tree is given [7].

2.1. Problem formulation

Given a set of n cores $B=\{b_0, b_1, \ldots, b_{n-1}\}$ and a set of m nets $N=\{c_0, c_1, \ldots, c_{m-1}\}$, the area of each $b_i \in B$ is A_i, the aspect ratio bounds are $[l_i, u_i]$, here l_i is low bound of aspect ratio while u_i is the high bound, and each core has its legal voltages. Assume that cores satisfy the timing constraint under the given legal voltage tables. Then, the corresponding power consumption can be calculated as follows. Let the power consumption of core b_i be $A_i v_i^2$, where v_i is the current working voltage selected from the legal voltages. For example, the cores information shown in Table 1 indicates that the area of core sb0 is 16 318, the aspect ratio bounds are [0.3, 3] and legal voltage levels are 1.0 V, 1.3 V and 1.5 V.

Then, the problem can be formulated as follows. Given a constant K and chip-level voltage V_c, a floorplan under a given fixed-outline with K VIs needs to be generated so that the total power consumption is minimized while chip area, wirelength and white space are optimized.

To further reduce power consumption, some strategies are proposed [31]. All the cores in the island are operated at the lowest common legal voltages while the remaining cores not belonging to any islands are supplied with V_c. By grouping the cores within the same inactive periods into an island based on the information from the dynamic behaviors of the cores with core states, active, idle or sleep, power can be further reduced by shutting down the island during idling. If the cores with similar inactive periods are grouped together as an island, then the additional power savings can be achieved. Take circuit n10 shown in Table 2 as an example. If sb0, sb1 and sb3 can be formed into an island, then an additional 30% power can be saved. Note that even if some of cores in the group are formed into an island, power can still be reduced. For example, if an island only consists of sb0 and sb1 and operates at v_i, then the power consumption is $(A_0+A_1)v_i^2 \times (1-30\%)$.

Table 1
Cores information and legal voltages table.

Cores	Area	Aspect ratio bounds	Legal voltages
sb0	16,318	[0.3, 3]	1.0,1.3,1.5
sb1	24,045	[0.3, 3]	1.0,1.3,1.5
sb2	7137	[0.3, 3]	1.2,1.5
sb3	19,038	[0.3, 3]	1.0,1.3,1.5
sb4	18,928	[0.3, 3]	1.3,1.5
sb5	26,832	[0.3, 3]	1.2,1.5
sb6	13,284	[0.3, 3]	1.1,1.3,1.5
sb7	42,065	[0.3, 3]	1.1,1.3,1.5
sb8	29,336	[0.3, 3]	1.2,1.3,1.5
sb9	24,696	[0.3, 3]	1.2,1.3,1.5