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High performance MEMS 0.18 μm RF-CMOS transformers

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ABSTRACT

This work presents the application of a front-side maskless MEMS process to improve the performance of RF-CMOS transformers. High-frequency parasitic effects are much diminished, as oxide and substrate material are etched away. The passivated metal surface prevents damage to the transformer, and to other circuits, which use metal layers as self-aligned etch masks. Device self-resonant frequency was improved by 20%. At 18 GHz, device quality factor rose from 0.5 to 6, and at 50 GHz, maximum available gain was increased by 49%. The process's low cost relative to other MEMS optimization methods with similar results makes this process attractive for the use of transformers in system-on-chip design.

1. Introduction

RF-CMOS monolithic transformers are used in RF-CMOS circuits such as voltage-controlled oscillators, mixers, power amplifiers and low-noise amplifiers, for purposes including impedance matching, converting between balanced and unbalanced signals, and achieving DC isolation.

Like spiral inductors, monolithic transformers are subject to a variety of parasitic effects. Series resistance in the transformer metal limits device quality factor (Q) at low frequencies. At higher frequencies, capacitances between the metal coils and between the coils and the substrate become significant. At high enough frequency, these capacitances form a parallel LC resonance with the coil inductance, causing a self-resonant frequency (f_{SR}) above which the coils no longer behave as inductors. Changing magnetic fields induce eddy currents in the resistive silicon substrate, which oppose the flow of current in the coils and lead to energy loss.

Various methods have been proposed to decrease the effect of these parasitic elements. In general, the degree of remediation achieved is inversely proportional to the cost of the process. At one extreme are the methods, which rely solely on CMOS layout choices. These methods include using multiple-level inductive coils to decrease series resistance [1], and introducing a patterned ground shield below the coil to block fields from entering the substrate [2]. These methods add no cost to chip fabrication, but their effect on parasitics is usually small. The patterned ground shield, for example, increases Q due to decreased substrate loss, but simultaneously decreases f_{SR} since the coil is closer to a conductor (the shield) and its shunt capacitance is increased.

At the other extreme are expensive methods involving complex micromachining, which are very effective at decreasing parasitic effects. These methods include various forms of non-CMOS substrate usage [3] and substrate transfer [4] or modification [5], as well as MEMS methods, which remove substrate and oxide material from around the transformer [6,7] or build new, suspended inductive structures above the chip surface [8]. The high cost of these methods, including additional process steps and the need for equipment not found in typical CMOS fabrication facilities, often prevents them from being cost-competitive as additions to a standard CMOS process.

In this work we present a MEMS method, which avoids many of the cost and complexity issues traditionally associated with the MEMS transformer optimization. CMOS-compatible post-processing is used so that no changes are needed in the chip fabrication process. Front-side rather than back-side etching is used, which eliminates the need for non-standard DRIE equipment since the necessarily etch depth and aspect ratio are much smaller. Front-side etching also avoids need for back-side mask alignment whose standard 0.18 μm CMOS mask aligners cannot perform. Micromachining is performed using CHF_3 and SF_6 dry etches, the first of which creates a passivation layer on exposed metal surfaces. This allows for a maskless process, as a top CMOS metal layer may be used as a built-in self-aligned mask, limiting micromachining to parts of the chip where inductors and transformers are located.

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All of these factors allow for a low cost MEMS process, which nevertheless achieves a level of performance comparable to that of more expensive transformer optimization processes.

2. Material and methods

A transformer was fabricated in a commercially available 0.18 μm RF-CMOS process from TowerJazz [9]. Its layout is shown in Fig. 1(a). One transformer coil had just one turn. The other coil consisted of two turns connected in parallel, effectively forming one turn. The low number of turns necessarily leads to relatively high f_{SR}, high Q, and low energy coupling between transformer terminals, independent of the choice of optimization process. The outer diameter of the outermost coil was 238 μm, the coil width 15 μm, and the gap between coils 2 μm. Except for underpasses, the transformer was implemented in the 2 μm-thick top CMOS metal layer. The interlevel dielectric (silicon oxide) layer had a total thickness of about 9 μm. The substrate used had a resistivity of 10 Ω-cm. A patterned ground shield was used in the "active" layer of the transformer design, improving the transformer performance before micromachining, but was mostly etched away by the micromachining.

A transformer after processing is shown in Fig. 1(b). The front-side micromachining process used essentially consists of just two

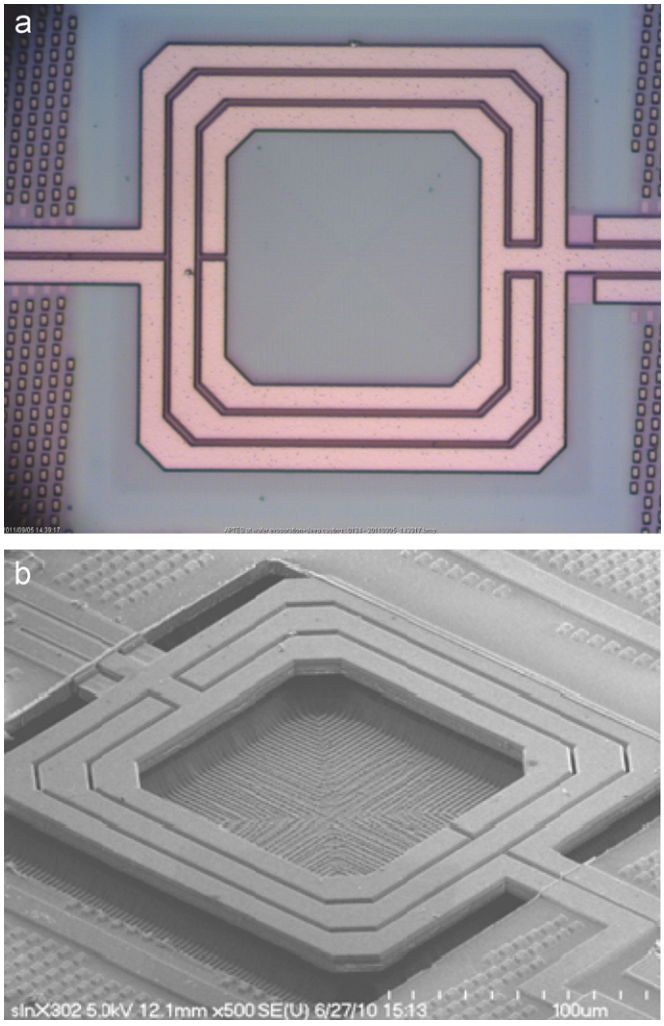

Fig. 1. Design of the transformer: (a) optical image of the transformer before processing; (b) fabricated transformer after micromachining: photo taken by SEM under 30° angle.

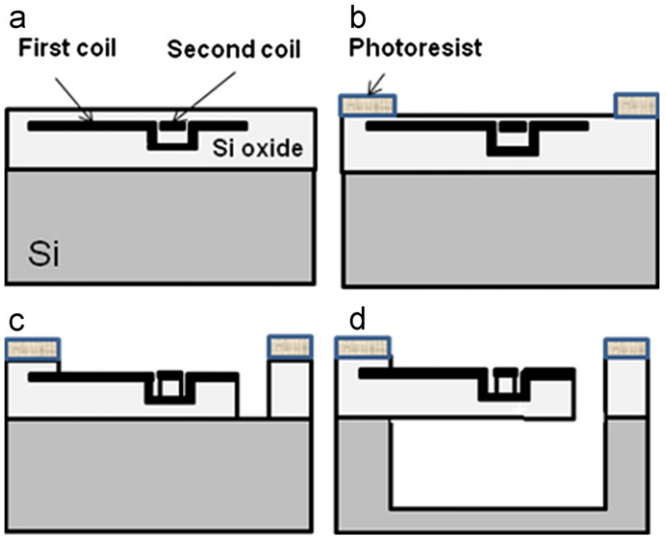

Fig. 2. Micromachining process flow: (a) starting point - standard CMOS die; (b) after photoresist deposition; (c) after oxide etching; and (d) after Si substrate etching. A cross-section along a transformer trace and including an underpass is shown.

etching steps, as shown in Fig. 2. First, a photoresist layer AZ 4562 is spun and patterned on the wafer to protect CMOS circuitry during the process. Then, an anisotropic CHF_3/O_2 (9:1) dry reactive ion etch (RIE) removes silicon dioxide from around the transformer, down to the level of the silicon substrate at an etch rate of about 2.5 μm/h. This etch forms a passivation layer on the aluminum surface of any metal layers encountered, protecting them from succeeding etching steps. The selectivity to the Al mask layer was better than 100:1. In the final step, an isotropic SF_6/O_2 (12:1) dry etch is used to remove substrate material from underneath the transformer. The isotropic etch was achieved due to the use of a relatively high gas pressure of 250 mTorr. The etching rate was about 50 μm/h. The allowable depth of this etch is limited by the action of SF_6 on the passivation layer and underpass connections, but substrate etching depths of 36 μm were achieved in this work, and deeper etching may be possible without causing device damage.

A possible intermediate etching step involves the application of a wet isotropic HF etch partway through the oxide etching process, once the metal of the top transformer layer has been exposed. In certain circumstances, the CHF_3 etch does not effectively penetrate into the narrow gaps between transformer coils, resulting in incomplete etching of the substrate and substantial diminishment of the benefits of micromachining. However, the necessity of this step depends on the conditions of the CHF_3 etch, and we have developed our process to the point where in general this step is unnecessary. In any case it must be run only for a short time, as the HF etch can attack metal as well as silicon dioxide once it reaches below the level of the CHF_3-deposited passivation layer.

The process is similar to that used by our group in [10].

3. Results

An Agilent E8361 vector network analyzer was used to obtain scattering parameter measurements of the transformer before and after micromachining. Two-port S-parameters were measured and de-embedded using a standard GSG SOLT calibration test pattern [11]. The S-parameters were then converted to Z-parameters and used to calculate inductance L, quality factor