Microelectronics Journal 44 (2013) 948–952

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

# Design and experimental results of a preamplifier for particles tracking in secondary electron detectors

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ARTICLE INFO

*Article history:*
Received 1 March 2012
Received in revised form
29 August 2012
Accepted 12 December 2012
Available online 6 March 2013

*Keywords:*
Preamplifier
Transimpedance amplifier
Particle tracking
Secondary electron detectors
Spatial detection
Radioactive ions beams

ABSTRACT

This paper presents the design and experimental characterization of a preamplifier used in the electronic front-end of low-pressure gaseous secondary electron detectors. The circuit—implemented in a printed circuit board as a proof of concept has been designed to cope with the specifications of the readout electronics used in spatial (beam particle position) measurements. Experimental results show a transimpedance gain of 80 dBΩ, an overall voltage gain of 18 dB, a peak signal-to-noise ratio of 36.5 dB and a shaping time frame of 140–170 ns. These features improve the performance of previous reported approaches to the problem, and allow us to minimize the overlapping probability in secondary electron detections for radioactive ion beams tracking, achieving a counting rate higher than $10^6$ particles per second.



## 1. Introduction

The next generation of particle accelerators will provide low energy Radioactive Ion Beams (RIB) with less than 10 MeV per nucleon and counting rates of $10^6$ particles per second (pps). The nuclear structure and reactions mechanisms of new isotopes will be studied; thanks to these beams. Ions track reconstruction (spatial and time detection) before target impact, are required to identify initial conditions of particles which produce a nuclear reaction. That track reconstruction requires suitable electronic readout systems for both spatial and time detection [1].

One of the most challenging circuits in these readout systems is the preamplifier. The design of this building block is specially critical due to its early position at the front-end interface connected to the detector [2]. An approach to implement the preamplifier is based on the principle of charge amplification, in which the preamplifier output voltage is a function of the input charge coming from the detector as well as the integration time and the value of the capacitor used to integrate the charge. These kinds of preamplifiers have been successfully applied in the past for experiments on CP violation of kaon particles at Low Energy Antiproton Ring (CPLEAR), and were developed at CEA-Saclay laboratories [3]. However, their performance may be severely degraded as the counting rate increases, which demands looking for alternative solutions [2].

This paper contributes to this topic and presents a 4-channel preamplifier system intended for spatial resolution measurements in a very specific kind of low-pressure gaseous detector [4], named Mini Secondary electrons Detector (Mini-SeD) [1]. The circuit—based on the combination of a TransImpedance Amplifier (TIA) and a shaper filter achieves faster operation than previous approaches and minimizes the probability of overlapping among signals coming from detected particles as the counting rate increases in beam tracking detectors. The system has been implemented in a Printed Circuit Board (PCB) and several experimental results considering different experiment conditions are shown to validate the preamplifier system presented in this paper.

## 2. System-level design

Fig. 1 shows a block diagram of the spatial detection system used in Mini-SeD detectors. The analog signal provided by a silicon detector and the anode output signal provided by the Mini-SeD are amplified and compared with a threshold voltage that must be higher than the system noise floor level in order to avoid capturing false events. This way, when a particle is detected, an active pulse known as "integration gate" is generated in order to set the integration time, as a first step to digitize the signal. A Charge-to-Digital Converter (QDC) is used as a digitizer in order to obtain the charge value at the output of the detectors

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http://dx.doi.org/10.1016/j.mejo.2012.12.009

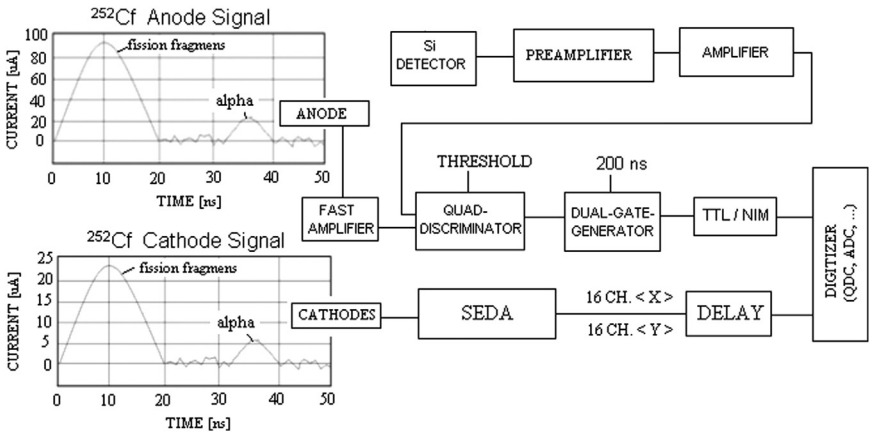


**Fig. 1.** Block diagram of the spatial detection system.

cathodes. This way, the charge distribution around *X* and *Y* axis cathodes constitute the two-dimensional spatial coordinates corresponding to a detected particle, also referred to as a valid event. The trigger indicates when an event takes place, i.e. when a particle is detected, and then, the QDC integrates a valid current provided by each channel of the preamplifier.

The proposed preamplifier, named Secondary Electrons Detector preAmplifier (SEDA) in Fig. 1, has been designed to process charge signals coming from Mini-SeD cathodes, tracking high counting rates of RIB with around 1 μs of average arrival time between two consecutive particles. Thus, when a particle is detected, current signal waveforms coming from cathodes have approximately a 10 ns rise/fall time. In order to relax the bandwidth specifications, these current signals waveforms are shaped so that they can be digitized by the QDC during an integration time period of 200 ns, which in our case corresponds to a 20% of the average particles arrival time. Another important design specification is the Signal-to-Noise Ratio (SNR), which should be high enough to discriminate signal currents peaks generated in the cathodes when particles are detected, typically in the order of tens of micro ampere.

One of the main limiting factors in Fig. 1 is the parasitic capacitance associated to the cable connections used in the experimental set-up environment. These parasitic may severely degrade the signal bandwidth and corrupt the detected signal due to the additional noise sources caused by the coupling effect of electromagnetic interferences. Therefore, the preamplifier should be placed as close as possible to the detector in order to minimize the impact of the mentioned parasitic. However, this is not always possible in practice due to spacing problems imposed by the vacuum chambers.

The preamplifier, implemented in a PCB in this work, has been designed to work outside the vacuum chamber. This forces using cables to connect each pre-amplification channel to the detector, with an associated input parasitic capacitance per channel of approximately 30 pF. In addition, a preamplifier connected directly to the detector, without using cables, has been simulated. In these simulations, the associated input parasitic capacitance per channel is approximately 4 pF due to the connectors.

Another important design restriction imposed by the spatial detection system is that the preamplifier output impedance should match with the cable input impedance and the connector impedance, 50 Ω in these cases.

## 3. Preamplifier architecture

Fig. 2 shows the schematic of one of the four (identical) channels of the proposed preamplifier. The system is composed of a TIA circuit, a shaper filter, an ac-coupled inverting amplifier and a line driver. An ElectroStatic Discharge (ESD) diode-based protection circuit is placed at the input node to avoid damages caused by high voltage sparks and other experimental set-up interference signals.

The preamplifier system in Fig. 2 has been implemented using commercial Integrated Circuits (ICs) as a proof of concept, as a previous step to design an ASIC. The different building blocks have been selected and configured in order to fulfill the system level performance in terms of voltage gain, transient response (characterized by fall- and rise-time) and SNR. To this purpose, a simulation-based top-down design methodology has been followed from system-level specifications to building-block specifications and final PCB implementation.

### 3.1. Transimpedance amplifier

The TIA building block in Fig. 2 was implemented using the AD8015 IC. Using a transimpedance of 10 kΩ, this circuit transforms the current signals coming from detector cathodes into voltage signals with a transimpedance gain of 80 dBΩ within a 240-MHz bandwidth, keeping the same rise/fall time and minimizing the probability of overlapping signals. In this configuration, this block has an input referred noise spectral density of 3 pA/$\sqrt{}$Hz—in good agreement with the overall SNR specification.

The effects of parasitic capacitance on both signal bandwidth and noise figure have been taken into account in the simulations. Thus, considering a 30 pF input parasitic capacitance due to the cable, the TIA output total noise power is 3.35 mV rms within a 32.7-MHz signal bandwidth. If a 4 pF input parasitic capacitance is considered, the overall TIA output noise power is 2.31 mV rms within a 87.7-MHz signal bandwidth.

### 3.2. Shaper filter

As stated in previous section, a shaper filter is needed in order to slow down the preamplifier output signal so that it can be digitized by the QDC and to minimize the output noise. To this purpose, a biquad filter configuration has been considered, made up of a RC High-Pass (HP) filter, a buffer and a second-order Low-Pass (LP) filter. The cut-off frequency of the RC HP filter was set to 50-kHz in order to reduce the TIA output offset error and flicker noise. Both the buffer and the biquad filter were implemented using LMH6733 operational amplifiers configured with 0 dB gain, yielding a shaping time lower than 200 ns—in agreement with system-level required performance.

Multiple simulations were carried out in order to find out the optimum performance in terms of SNR, rise/fall time and cut-off