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Analysis of integrated circuits thermal dynamics with point heating time

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ABSTRACT

The article presents an analysis of thermal dynamics in integrated circuits using a new method. The introduced variable that defines the dynamic state of an IC is point heating time (PHT). The authors examine the dynamic behaviour of the integrated circuit caused by the thermal activity of one and many functional modules on the multi-core chip. Various substrate materials were analysed and the PHT value was compared to the mean temperature of the integrated circuit and its time constant. The PHT value is also analysed as a variable dependent on the distance from the heat centre of the heating module. The analytical equation, which is a result of the analysis, can describe the PHT value versus distance for the whole chip surface. Further analysis helps verify the hypothesis using a massive multi-core integrated circuit. The result can be used to increase the thermal efficiency of multi-core integrated circuits by thermal-aware flow modification of the scheduling algorithm.

1. Introduction

The current trend in the modern multi-purpose processor design leads to the development of multi-core universal processing units [1]. The design principle is to place many functionally identical, independent processing units on one die. This may help sustain the Moore Law principle, because nowadays there is no visible roadmap for implementing more "frequency powered" processors [2,3]. All of this has led to the production of, e.g., Intel Core i7 [4] processor (Fig. 1), future (in laboratory tests) designs like 80-core Intel Polaris [5] (Fig. 2) and IBM/Toshiba CELL processor [6] (Fig. 3). Despite the complicated internal structure, designers can determine power consumption for a whole chip surface. Unfortunately in this case, when the chip consists of many independent modules on a rather substantially large chip, the thermal aspects still are difficult to keep on acceptable levels [25–27]. These aspects are connected with the processor's work in order to achieve the maximum performance rating near a thermal boundary of the integrated circuit for a given technology and simultaneously the maximum temperature does not exceed the critical thermal level. The thermal design and its influence on the chip do not currently take into account the dynamic aspect of thermal simulations.

An additional factor that has increasingly significant impact on the computation capabilities of integrated circuits is their thermal restrictions. The actual design of integrated circuits needs an effective heat dissipation method. Because of that, designers include even more complicated active thermal cooling techniques. For the most popular CMOS process, the thermal boundary is set at 125 °C [7]. The active cooling mechanism reacts to temperature changes considerably later just after the time of the cause. A steep temperature rise on the surface of the chip (generated by e.g. increased activity of the computation module) is not likely to be neutralized by passive and active cooling. This is the main reason for decreasing the working temperature for all current processor designs to acceptable levels by a cooling mechanism. The main goal for this paper is to present a new method to analyze the dynamic thermal behaviour of the multi-core integrated circuit.

In the published paper [8], partitioning dissipation of power into dynamic and static power losses emphasizes the rising impact of the latter's value on total power. Nonetheless, in [9] the authors presented an analysis showing that in current evolution in microelectronics research, dynamic power will still have considerable influence on the total power loss in an integrated circuit. It is a strong justification to do research on minimizing dynamic power loss and its influence on the thermal working boundaries for integrated circuit design. Many researches were made in order to minimize total power dissipation. The most popular techniques include dynamic voltage scaling [10–15] and dynamic frequency scaling [16–19]. Dynamic power loss [20] is described as

$$P_{dyn} = fC_L V_{DD}^2 \quad (1)$$

where f is the chip working frequency; C_L is load capacity; and V_{DD} is supplied power.

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Based on thermal analysis, the authors proposed a novel method for asynchronous control of functional module activity in an integrated circuit. In [21], the authors present an example mechanism of activity control in order to minimize maximum peak temperature of an integrated circuit. The switching frequency of the integrated circuit module activity influenced the peak temperature. Let us stress that the switching frequency determines the switching between the active and passive modes of an integrated circuit module—and not the working frequency of an integrated circuit. Additionally, the algorithm introduced switching between the modules in order to spread the thermal activity all over of the surface of an integrated circuit. The example mechanism that consists of switching between cores is presented visually in Fig. 4. The activity is spread to the available cores.

As stated in [21], the temperature caused only by the active power dissipation during activity switching conforms to the equation

$$T \sim \frac{1}{\sqrt{\omega}} \tag{2}$$

where T is the temperature and ω is the pulsation of the switching activity $\omega = 2\pi f$. Visually, the activity switching method can be shown as in Fig. 5. Asynchronous activity switching occurs when the temperature of an integrated circuit is over some defined level—as seen in the picture: the over-temperature area.

Because of these there is a strong demand to estimate and define the dynamic power loss in real time. The best solution is to estimate not only current power loss but also on the basis of computer flow to be able to predict and control power dissipation before real damage can be caused on the hardware level.

In order to define dynamic thermal behaviour of an integrated circuit, a corresponding variable has to describe dependencies that connect physical components of the integrated circuit with its thermal response to a test pattern [22]. The proposed dynamic change is a value that can describe the influence of one thermal active module on the total chip temperature and its dynamic change during computation of the stream of data. In order to investigate thermal dynamics of any integrated circuit, point heating time (PHT) value will be introduced. The PHT value allows us to compare physical and thermal properties of an integrated circuit. The next section will cover the PHT definition and method of its calculation from the initial thermal simulation data.

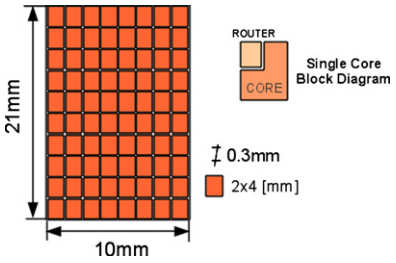

Fig. 1. Massively multi-core processor Intel Polaris (80-core).

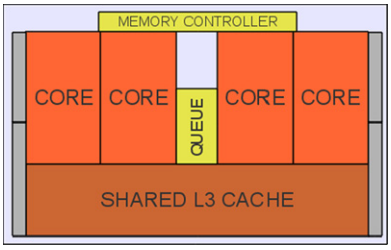

Fig. 2. Intel Core i7.

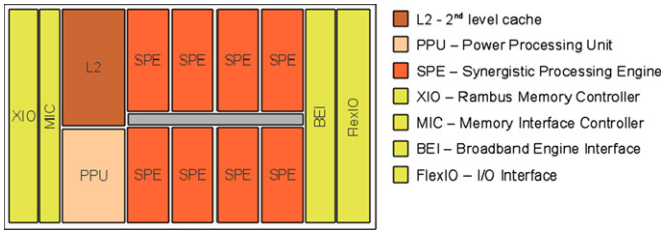

Fig. 3. IBM, Toshiba, Sony: CELL.

2. Point heating time

The point heating time (PHT) value is the duration of temperature growth in any measurement point in the chip volume, which is caused by a heat source located on the chip surface. When we assume that an integrated circuit/micro-circuit temperature reaches its stationary state in the time 3τ, τ is the point heating time value for mean temperature [23]. This value is derived from the equation that describes a mean temperature on the integrated circuit [22].

$$T_m(t) \approx \frac{\sum_N^{i=1} P_i}{2\alpha L_x L_y} \exp(-t/\tau) \tag{3}$$

where

$$\tau \approx \frac{\rho c L_z}{2\alpha} \tag{4}$$

and T_m is the mean temperature of an integrated circuit; P_i the power dissipated by the core number 'i'; τ the time constant; ρ the density of the material; c_v the specific heat; L_x L_y are the dimensions of an integrated circuit; L_z the chip thickness; α the generalized convection coefficient; t the time; N the core count.

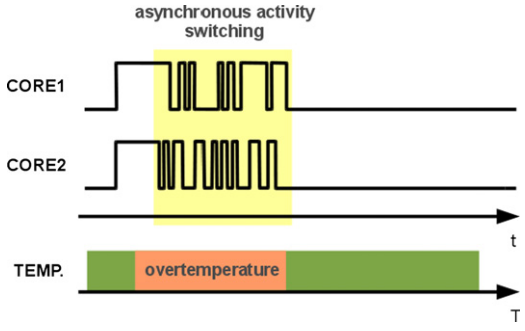

Fig. 5. Activity switching example (TEMP.—maximum core temperature).

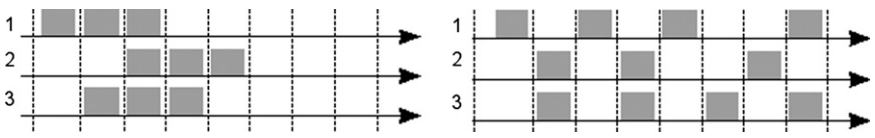

Fig. 4. Module switching—diagram of switching.