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Cu/barrier CMP on porous low-*k* based interconnect schemes

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Abstract

Dielectric stacks containing porous low-*k* materials were investigated regarding their ability to pass CMP processes as used in Cu interconnect technology. Beside the low-*k* material itself, the impact of layout, cap layer materials and different diffusion barrier materials has been proven. Advanced consumables, partly specially designed for future technology nodes, have been tested within these experiments. Compatibility of the slurries with the low-*k* stacks, dishing and erosion, impact of polishing parameters like down force and platen speed on low-*k* stack integrity were examined. Low-*k* stacks based on a porous MSQ material capped with PECVD-SiC or with a MSQ-hard mask were found to be promising candidates. Low-*k* stacks based on porous SiO_2-aerogel could not meet the stability requirements at present and need additional efforts for adhesion enhancement between cap layer and porous material. Consumables used within the experiments enable an efficient processing with low dishing and erosion as well as an excellent surface quality.

Keywords: CMP; Cu/barrier CMP; Low-*k*; Low-*k* material; Low-*k* dielectrics; Porous low-*k* materials; Damascene architecture

1. Introduction

Interconnect schemes for high performance ICs like microprocessors use Cu interconnects embedded in dielectric materials with a low dielectric constant separated by a diffusion barrier in dedicated metal levels [1,3]. Against the background of a continuously increasing integration density by an ongoing shrinking of feature sizes, such interconnect schemes ensure performance and reliability of the IC. The fabrication of Cu interconnects uses the damascene concept which involves a chemical mechanical removal (polishing) of the waste metal [2–4].

In contrast to the excellent electrical behavior of low-*k* dielectrics, their mechanical properties lead to some challenges, especially for their integration in multilevel interconnect schemes. Low-*k* dielectrics are characterized by a significantly lower E-modulus compared to other dielectric materials like SiO_2, PSG, and BPSG. In general, this leads to a lower mechanical strength. Porous low-*k* materials, as proposed for the 45 nm technology node and below, intensify that challenge [3]. The lower adhesion of low-*k* dielectrics to adjacent materials is a further known issue. The aforementioned issues have to be addressed especially for Chemical Mechanical Polishing (CMP), because of the high mechanical impact of that technology. Consequently, Cu/barrier CMP processes need to be adapted, developed, and tested when applied together with (porous) low-*k* materials.

This work summarizes a series of experiments to define CMP processes which enable damage-free and effective polishing of Cu interconnects using porous low-*k* materials. Thereby, advanced consumables (partly research grade) have been tested. Different low-*k* stacks based on two porous low-*k* materials in conjunction with several cap layers were included in these experiments to figure out suitable material combinations.

2. Experimental

2.1. Equipment and materials

Experiments have been carried out on an Applied Materials Mirra™-polishing tool. Post-CMP cleaning was done

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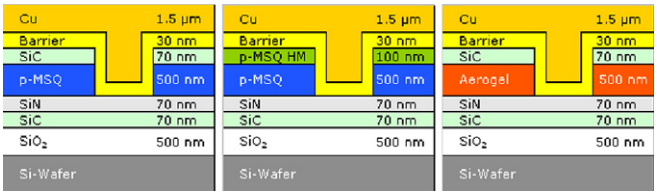

Fig. 1. Schematics of single damascene interconnect based on p-MSQ and SiO_2-aerogel as used in the CMP experiments.

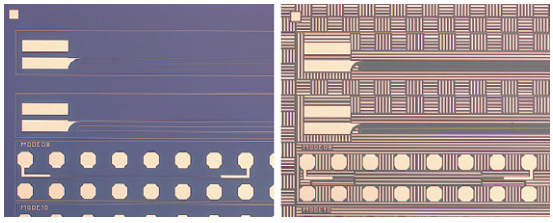

Fig. 2. Different layouts used within the CMP investigations.

using an OnTrak DSS 200 scrubber. Single damascene metallization samples have been prepared on six inch wafers using different low-*k* stacks as shown in Fig. 1. Layouts with and without dummy patterns were included to investigate their impact (Fig. 2).

Both low-*k* materials were processed using a spin-on technology. The MSQ material has a porosity of about 30% exhibiting a mean pore radius of 2.1 nm. The porosity of the SiO_2 aerogel is about 50%, the mean pore radius is 3–4 nm. PECVD-SiC and spin-on MSQ-based **H**ard **M**ask films were used as cap layer. Sputtered Ti/TiN/Ti and Ta/TaN/Ta films have been applied as barrier. Cu was electrochemically deposited onto a sputtered Cu seed layer.

Possible chemical interactions between slurries and low-*k* materials (material stacks) have been investigated using blanket low-*k* samples (Fig. 3). These samples were characterized by optical inspection and electrical measurements (leakage current, break down field strength, *k*-value) after preparation and after slurry treatments of 1 min and 10 min, respectively.

2.2. Consumables

Polish pads and chemicals provided by Rohm and Haas Electronic Materials were used and tested within these CMP experiments. Specific properties of the chemicals summarizes Table 1. The used polish pads were CUP4410™, IC1010™, and Politex™. In contrast to the k-grooved IC1010™ pad, the CUP4410™ pad combines k- and x-y-groves as shown in Fig. 4. Both pads were tested for Cu bulk removal as well as for Cu clearing. The Politex™ soft pad was used for barrier removal.

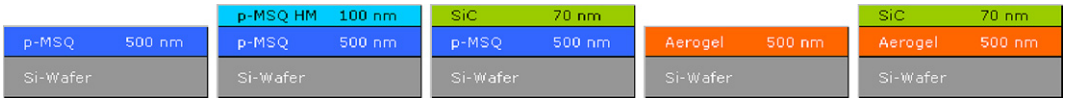

Fig. 3. Blanket low-*k* samples to characterize possible chemical interaction between slurries and low-*k* materials.

Table 1
Selected properties of chemicals used within the CMP experiments

	Epoch Cu bulk slurry	RHEM Cu clearing slurry	RHEM barrier slurry	Epoch pad cleaner
Purpose	Cu bulk removal	Cu clearing	Barrier removal	Pad cleaning
Abrasive type	Colloidal silica	Particle free	Colloidal silica	Particle free
Abrasive size	<50 nm		<30 nm	
Oxidant	H_2O_2	H_2O_2	H_2O_2	
pH-Value	4.0–4.4	2.6–2.6	2.7–3.0	1.0–2.0

Fig. 4. Groove layout of CUP4410™ (left) and IC1010™ (right) polish pads.