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Design investigation of nanoelectronic circuits using crossbar-based nanoarchitectures

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ABSTRACT

Nanowire crossbar is an efficient nanoscale architecture which can be used for logic circuit design. In this work, we study and compare different crossbar nanoarchitectures and their application in logic circuit implementation. To evaluate the performance of crossbar architecture compared to the conventional CMOS logic design, we have implemented logic circuits using both approaches. The equivalent circuit models of the crossbar-based circuits are then extracted and simulated using HSPICE. The CMOS circuits are also simulated using 22-nm technology parameters. Our simulation results show that crossbar-based circuits have much smaller area while CMOS circuits show better performance in terms of delay. We implemented area optimized cell libraries based on the crossbar architecture which considerably reduces circuit area. Simulation results of benchmark circuits using SIS synthesis tool indicate that the crossbar cells can be combined with CMOS cells to achieve tradeoff between circuit area and speed.

1. Introduction

Today's semiconductor industry uses photolithography techniques to transfer design patterns onto silicon wafers. While CMOS based structures are scaling down in order to maintain the anticipation of Moore's Law, they face challenges due to the quantum effects and manufacturing issues [1]. Today, it is accepted [2] that current lithographic patterning can be hardly used in few nanometer scales, and hence, there is rapidly growing interest in the nanoscale technology to construct memories and logic circuits. There is large interest toward emerging technologies as a replacement of the CMOS technology. These technologies are divided into two sets from a physics point of view [3]: those that are based on the physics similar to CMOS, such as carbon nanotubes (CNTs) and silicon nanowires (SiNWs), and those with different physics, which includes spintronics [4], quantum cellular automata (QCA) [5,6], single electron transistors (SET) [7,8], molecular electronics, DNA and biological computing [9].

One of the most promising nanoscale paradigms is the nanoarray architecture, especially the nanowire crossbar. The nanowire crossbar is a two-dimensional array (nanoarray) consisting of two orthogonal sets of parallel nanoscale wires, such as CNTs and SiNWs [10]. In such architectures, any intersection or crosspoint of two wires within the crossbar architecture can be configured as an electronic device, such as a resistor, a diode, or a transistor. These structures have some favorable characteristics such as small size, high density, and periodic geometry, making them good candidates for the upcoming high-density interconnect and logic circuits implementation [10–14]. Various nanoscale architectures, such as NanoFabric [15], NanoPLA [16], NASIC [17], CMOL [18], 3D nFPGA [19], FPCNA [20] and RDG-CNFET [21], are introduced in the literature. These architectures have different structures, physical parameters, design strategies and fabrication processes, which cause them to have their advantages and disadvantages. The nanowire crossbar has been used in memory architectures because of its periodic structure [13,22]. Although, currently it is not possible to make an electronic circuit by using nanoscale devices, but combining it with CMOS circuits may be considered an interesting idea [23].

In this paper, we have investigated different nanoscale crossbar architectures in terms of their characteristics and properties. Among these, the architecture introduced by HP is the one that was used to physically implement logic circuits [24]. Although, some works have addressed the use of nanowire crossbar architecture for logic implementation [12,24,25] but their performance cannot be evaluated compared to MOSFET circuits. We have implemented some logic circuits using both MOSFET and CMOS-like crossbar architecture to compare their performances in terms of delay and area. The rest of this paper follows with a brief description of crossbar architectures and related technology, which are given in Sections 2 and 3. The nanowire crossbar proposed in Ref. [26], which we have used for our simulations, is described in Section 4. Performance evaluation of

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nanowire crossbar and simulation results are presented in Section 5, and finally a summary and conclusion are given in Section 6.

2. Nanoscale technology

This section gives a review of the nanoscale fabrication technologies. Then, different types of nanoscale devices and nanoscale crossbar architectures including related issues are explained.

2.1. Fabrication technologies

There are two main approaches to fabricate nanostructures; bottom-up and top-down techniques. In the top-down approach, which is currently employed in the silicon industry, devices such as transistors are etched on silicon wafers using the photolithography process. The physical dimensions of these devices are limited by the resolution of the lithography method. Standard photolithography techniques along with accurate control of etching, oxidation and deposition can be used to define small features. The electron-beam lithography is another way to achieve higher resolution than standard photolithography. The spacer patterning technique (SPT) is another top-down technique which exploits photolithography and anisotropic etch of the deposited materials to transform vertical features in the vicinity of a step of a sacrificial layer into horizontal features [27,28]. In Ref. [29] the multi-spacer patterning technique (MSPT) is used to build poly-Si nanowire FETs, which can be put in the crossbar architecture. Alternative techniques use nanoimprint lithography (NIL), in which a nanomold is pressed onto a resist-covered substrate to create desired pattern [30].

As an alternative, bottom-up techniques can be used to implement emerging technologies with nanowires and carbon nanotubes. In the bottom-up approach the devices and the nanowires are synthesized first, and then assembled into functional devices and systems. Different chemical assembly methods including Langmuir–Blodgett films [31–33] flow-based alignment, random assembly, biologically assisted assembly, and catalyzed growth can be used in bottom-up process [34,35]. The assembly can be controlled on an atomic or a molecular scale and hence size limits could be much smaller. Generally, the bottom-up assembly approaches can only produce structures with extreme regularity and high defect rates [36]. One of the bottom-up techniques is the vapor–liquid–solid (VLS) process [37,38], in which crystal growth occurs from the nucleated catalytic seed at the metal–solid interface.

2.2. Nanoscale wires and devices

Two major wire types, CNTs and SiNWs, can be distinguished in nanotechnology. CNTs can be synthesized in nanometer scale, but we cannot control the detailed electrical properties for these nanotubes. SiNWs are other promising building blocks for nanoscale computing systems. The electrical properties of these SiNWs can be controlled with dopants, resulting in semiconducting wires. NWs can be used along with nanotubes, in which their properties complement each another.

The nanowires can be fabricated in two forms: *undifferentiated* or *uniform* nanowires, and *differentiated* or *encoded* nanowires [1]. The uniform nanowires are grown identically, with no specific doping profile, and are differentiated after assembly. The *differentiated* nanowires are grown with different encodings in advance, which results in a certain doping profile. Dopant molecules are added to a gaseous mixture as the nanowires grow. As a result, heavily and lightly doped regions form along the nanowire lengths, depending on the exposure time as shown in Fig. 1a. These two types of nanowires can be used as active devices in different ways. Consider a microwire (MW) at the top of a uniform nanowire. Depositing impurities such as gold particles or depositing a high-κ dielectric at the contact between the microwire and nanowire can lead to a controllable junction, and preventing the deposition of such impurities makes the junction uncontrollable. Applying an electric field on the microwire can control the conductance of the nanowire [39]. A schematic view of such device is shown in Fig. 1b.

3. Nanoscale regular architectures

Semiconductor nanowires (NWs) can be made using different materials including silicon [40], germanium [39], InSb [41], etc. It is possible to assemble these materials into regular arrays using assembly techniques. The crossbar shown in Fig. 2 is a simple network consisting of two orthogonal sets of parallel nanowire layers separated by an interlayer [24]. The interlayer between the two planes of parallel nanowires determines the type of devices that will be configured. Any intersection or crosspoint of two wires within the crossbar can be configured as an electronic device, such as a resistor, a diode, or a transistor; hence, various crossbar circuits are possible. Crossbars can be used to implement interconnect networks, memories, and logic circuits as well (e.g., [12,22,42]).

Various crossbar based architectures are introduced in the literature. In a diode-based crossbar, each crosspoint can be configured as a diode or to an open circuit after fabrication. Though this structure has some inherent limitations, it may be used to implement memory units and logic circuits [25]. Several works have been proposed to build FETs out of carbon nanotubes [43] or silicon nanowires [44]. In the nanowire approach, one nanowire can act as the gate of the transistor to control the other crossing nanowire which forms the source and the drain of the transistor. Using these types of transistors one can build logic gates [12]. Some works have addressed the use of memristors as crosspoint devices to build crossbar architectures [45], as explained in the following subsections. Although all the architectures have crossbar structure, they use different devices and fabrication technology.

3.1. NanoFabric

NanoFabric, which is proposed by Goldstein and Budiu, is based on the chemically assembled electronic nanotechnology (CAEN) [15].

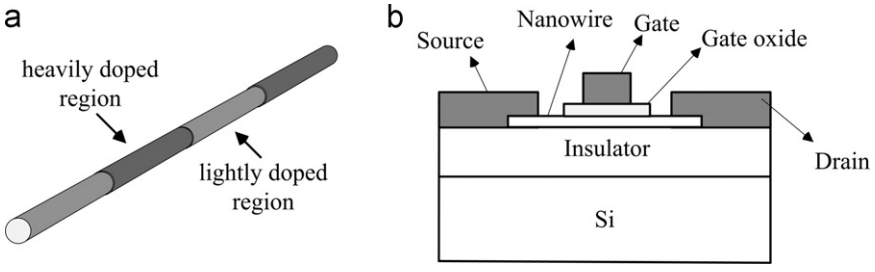

Fig. 1. (a) Encoded nanowire, (b) Schematic of a NWFET device with high-κ dielectric layer.