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Current mode read-out circuit for InGaAs photodiode applications

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ABSTRACT

Infrared focal plane arrays have many military, industrial, medical, and scientific applications that require high-resolution and high-performance read-out electronics. In applications involving InGaAs sensor arrays, data read-out can be carried out by circuits implemented with 0.35 μm CMOS technology. In this paper we propose a dynamically regulated cascode current mirror for pixel read-out. From simulation results, we expect this circuit to achieve a better trade-off between silicon area, signal-to-noise ratio, and output dynamic range than the trade-off that is currently achieved by current mode CMOS read-out circuits.

1. Introduction

The design of read-out integrated circuits (ROICs) for infrared image sensors [1–6] is similar to the design of ROICs for visible light image sensors [7–13]. Many (infrared) focal plane applications exist—military, industrial, medical, and scientific—in which high-performance read-out electronics and high-resolution are simultaneously required. There is a conflict between these requirements: increasing the number of pixels and keeping the overall chip area constant will reduce the complexity and therefore impair the performance of the ROIC.

The performance of a current mode ROIC involves the following desirable properties: well-controlled bias point, low noise, low input impedance, and high dynamic range:

- The accurate bias point and the low noise reduce the smallest detectable signal, taking into account the minimum light level that is set by the photodetector dark current [14].
- A lower input impedance contributes to a higher injection efficiency [3], so that the same integration capacitor can be used to implement a detector with larger bandwidth.
- A larger dynamic range leads to an increase in the maximum stored charge, for the same integration capacitance. If large integration capacitors must be used, they should be placed outside the pixel as shown in Fig. 1. This figure, which represents a typical application of current-mode read-out circuits, conveys the idea that the current mode is usually restricted to the pixel area, and the distribution (multiplexing) of pixel samples is accomplished in voltage mode.

Most of the reported ROICs are implemented in voltage mode. In this case, the voltage mode is also used in the pixel area. In either case—current-mode pixel or voltage-mode pixel—all pixels share a common architecture for the implementation of column and row addresses for array read-out. This architecture, which is often implemented in voltage mode regardless of the pixel mode, is shown in Fig. 2. When analog-to-digital converters are used, they often digitize the integrated current at the output of the column amplifiers. As the minimal transistor channel length becomes smaller in CMOS technologies, the supply voltage is reduced. This impairs the output dynamic range of the column amplifiers.

By contrast, the output dynamic range of current-mode read-out amplifiers is not impaired by the reduction of the supply voltage. A current-mode ROIC is easily integrated with current-mode image processing circuits, so that an image can be processed in analog domain, i.e. before digitization takes place. Depicted in Fig. 3, this idea has been known for some years as *smart pixels* [15–19]. Current-mode image processing circuits use simpler building blocks and have higher operation speed than their voltage-mode counterparts. The ROIC must have a very high output impedance, and the integration of current signals into read-out capacitor voltages does not happen.

In this work we propose two current-mode amplifiers for ROIC applications. Using electrical simulations, we compare the proposed circuits with state-of-the-art ones. We present a

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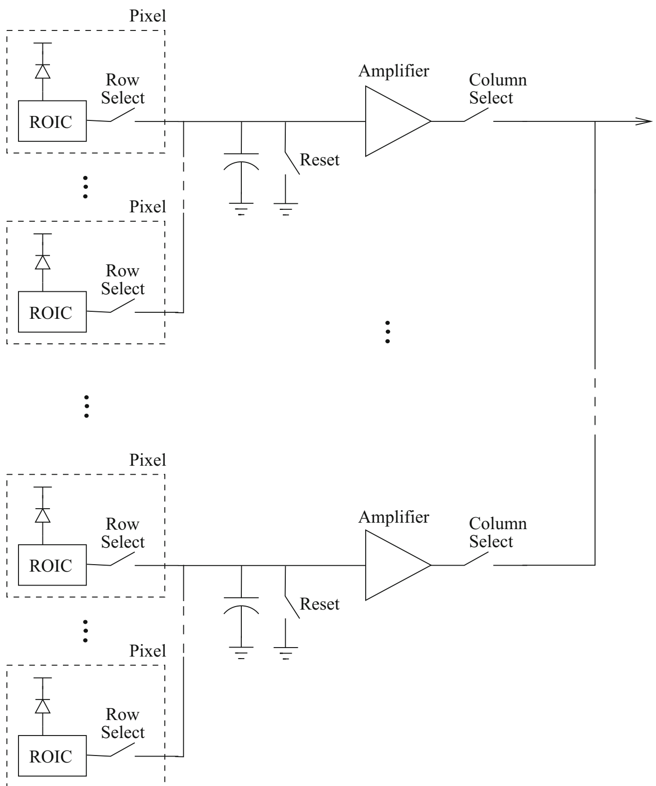

Fig. 1. Typical application of current-mode read-out circuits. Note that the current mode is restricted to the pixel area. Pixel samples are actually read-out of the sensor array in voltage mode.

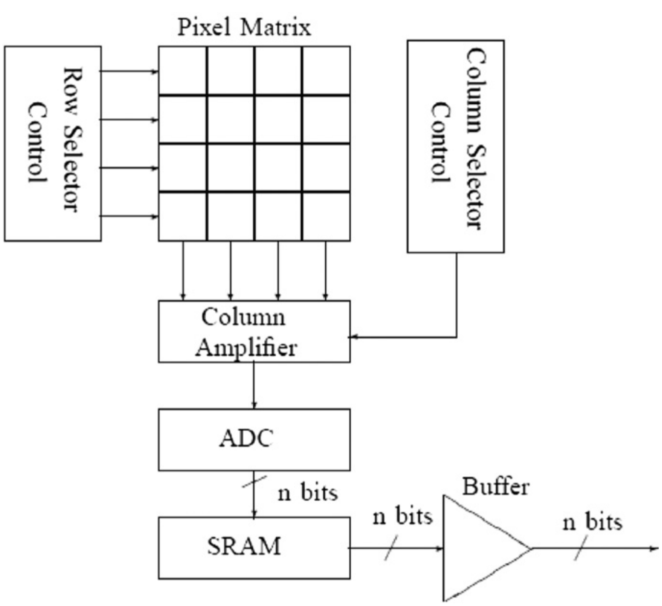

Fig. 2. Array architecture for the implementation of read-out schemes based on row and column addresses. Pixel samples are usually represented in voltage mode, regardless of pixel inner circuits being current-mode or voltage-mode.

state-of-the-art review in Section 2, and a model for the InGaAs infrared photodiode in Section 3. The regulated cascode current mirror and the dynamically regulated cascode current mirror are introduced in Section 4. In Section 5, noise and harmonic distortion performance figures are computed for both circuits. Post-layout electrical simulations with BSIM3V3 models are presented in Section 6, and the conclusions are presented in Section 7.

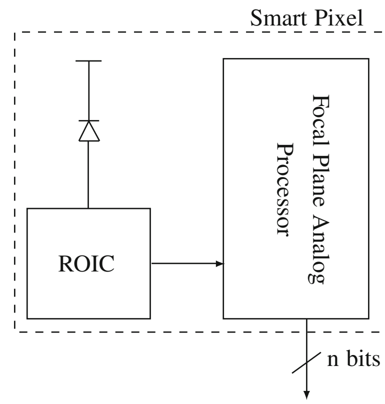

Fig. 3. Application of current-mode read-out circuits for current-mode focal plane image processing.

2. State-of-the-art review

InP–InGaAs infrared sensors have been considered as potential alternatives to low bandgap semiconductor infrared photodetectors such as HgCdTe. HgCdTe photodetectors suffer from (responsivity nonuniformity) at the infrared band, and the InP-InGaAs alternative offers long-wavelength infrared arrays at a significantly lower cost [6]. A disadvantage of InP–InGaAs techniques for infrared applications is their lack of flexibility: it is difficult to adjust the peak detection wavelength by changing the barrier/well material composition. As a consequence, the peak responsitivity is limited to a narrow band around 8 μm [20].

An InGaAs photodiode can be easily modelled as a silicon photodiode. The design of a ROIC for CMOS technology can be copied in a straightforward manner [21] for a hybrid CMOS-InGaAs implementation—the photodiodes are implemented in InGaAs technology and the CMOS ROIC is connected to the photodiode array by means of flip-chip indium bonds.

The majority of the reported ROICs is implemented with the three-transistor active pixel sensor (APS) topology [7–13]. This topology has three elements: (i) a voltage amplifier (for voltage mode applications) or a transconductance amplifier (for current mode applications), (ii) a switch for resetting the photodiode voltage level at the beginning of a charge integration period (also in current mode), and (iii) a switch for row or column read-out. This topology is associated with techniques such as self-integration, one source follower per detector, and direct injection [2,4–6].

More recent amplifier structures, such as buffered direct injection and capacitive feedback transimpedance amplifier, provide a better performance in terms of injection efficiency and detector bias stability [5], with the help of an in-pixel operational amplifier. However, their performance is limited by the performance of the operational amplifier that can be implemented in the pixel area. Another technique, known as buffered gate modulation input [5], provides in-pixel detector current amplification and current-mode background level suppression. The integration capacitance is placed outside the pixel, but an operational amplifier is still required for detector bias stabilization. Another interesting technique is switched current integration [6]: it provides a large storage capacity by means of an off-pixel integration capacitor. However, this technique still requires an in-pixel operational amplifier. A technique known as current mirroring direct injection [3] satisfies the requirements of high injection efficiency and detector bias stability, but an in-pixel integration capacitor is used, which impairs pixel area, dynamic range, and charge storage capacity. Finally, in [2], the authors achieved high-performance (i.e. stable bias point and high injection efficiency) without using neither an in-pixel operational