Microelectronics Journal 41 (2010) 417–429

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

An IEEE 1149.1-based BIST method for at-speed testing of inter-switch links in network on chip

Reza Nourmandi-Pour [a,*], Ahmad Khadem-Zadeh [b], Amir Masoud Rahmani [a]

[a] Islamic Azad University, Science and Research Branch, Tehran, Iran
[b] Iran Telecommunication Research Center, ITRC, Tehran, Iran

ARTICLE INFO

Article history:
Received 26 September 2009
Accepted 26 April 2010

Keywords:
BIST
IEEE 1149.1
Interconnects
Crosstalk
NOC
Link

ABSTRACT

With advance in technology and working frequency reaching gigahertz, designing and testing interconnects have become an important issue. In this paper, we proposed a BIST-based boundary scan architecture to at-speed test of crosstalk faults for inter-switch communication links in network on chip. This architecture includes enhanced cells intended for MVT model test patterns generation and analysis test responses. One new instruction is used to control cells and TPG controller in the at-speed test mode in order to fully comply with conventional IEEE 1149.1 standard.

1. Introduction

1.1. Motivation

Nowadays with advance in VLSI technology, designers are capable of embedding the components of a system in a single chip in the shape of functional and storage cores. These chips, called system on chip (SOC), can include a series of heterogeneous components with irregular block sizes or homogeneous components with regular block sizes. SOC designing methodology, today, has undertaken basic changes, which is due to emergence of SOC platforms, which support large complex of embedded cores [1]. In this type of chips, exchanging data between cores is done through a dedicated communication infrastructure (e.g. shared bus structure). Low scalability of the bus structures and increasing in chip operation complexity posed some limitations to designers to embed too many cores in SOCs. Therefore, a key requirement of these platforms, whether irregular or regular, is a structured communicational architecture. Network on chip (NOC) architectures were proposed as a holistic solution for a set of challenges faced by designers of large multicore SOCs. Communication infrastructure for NOC includes switches and inter-switch links. Functional and storage cores connect to this infrastructure via network interfaces and exchanging data between cores is performed according to a protocol.

Any new design methodology will only be widely adopted if it is complemented by efficient test mechanisms. The test strategy for NOC-based systems addresses three problems: testing the functional and storage cores and their corresponding network interfaces, testing the communication infrastructure itself, and testing the integrated system [2]. Since the inception of SOC designs, the research community has targeted principally the testing of the cores, giving little emphasis to the testing of their communication infrastructures. The main concern for SOC test was the design of efficient test access mechanisms (TAMs) for delivering the test data to the individual cores under constraints such as test time, test power, and temperature. Among the different TAMs, TestRail [3] was one of the first to address core based tests of SOCs. With the appearance of the NOC architecture, recently, a number of different research groups suggested the reuse of the NOC communication infrastructure as a TAM [4–9]. They assumed the communication infrastructure is fault-free and subsequently used it to transport test data to the functional blocks; however, for large systems, this assumption can be unrealistic, considering the complexity of the design and communication protocols.

With fine miniaturization of the VLSI circuits, existence of long inter-switch links in communication infrastructure of NOC and rapid increase in the working frequency (currently in gigahertz range), signal integrity has become a major concern for design and test engineers. Use of nanometer technology in NOCs magnifies cross-coupling and mutual inductance effects among the wires of the link. This phenomenon, which is known as crosstalk, affects the integrity of a signal by adding noise and delay. Various

* Corresponding author.
E-mail address: noormandi_r@srbiau.ac.ir (R. Nourmandi-Pour).

0026-2692/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2010.04.014

parasitic factors such as parasitic capacitances, inductances and their cross-coupling effects on the wires are difficult to control during fabrication. Moreover, the impact of process variation on circuit operation is an important issue in deep submicron (DSM). Process variation and manufacturing defects both may lead to unacceptable levels of noise and delay. The goal of design for DSM is to minimize noise and delay. However, it is impossible to check and fix all crosstalk effects during DSM design by only design rule checking (DRC), validation and analysis. Process variations and manufacturing defects may lead to unexpected changes in coupling capacitances and mutual inductances between wires. They in turn result in loss of signal integrity (e.g. glitches and excessive delay, which are referred as crosstalk faults), which may eventually cause logic error and failure of the chip. The impact of spot defects and process variations on the magnitude of inductance induced noise are reported in [10]. The authors reported that the maximum crosstalk pulse considering process variation is almost twice the value for the nominal set of parameters. Since it is impossible to predict the occurrence of defects that cause noise and delay, crosstalk testing is essential to ensure error-free operation of the chip and must be addressed in manufacturing testing. Therefore, we need a mechanism to coordinate activities in a crosstalk test session. We believe that one of the best choices is the boundary scan test methodology that includes the capability of accessing wires of the link. Boundary scan test methodology was initially introduced to facilitate testing interconnects among components of system on board (SOB). The IEEE 1149.1 Boundary Scan Test standard [11], also known as Joint Test Action Group (JTAG) Standard, has been widely accepted and practiced in the testing community. The standard provides excellent testing features with low complexity but it was not intended to address at-speed testing of crosstalk faults. The standard, nevertheless, can provide a mechanism to test core logic and the bus structure shared among them in SOCs and/or to test the inter-switch links in NOCs. However, the bus and the links can be tested for stuck-at, open and short faults [12]. In this paper, we extended the IEEE 1149.1 boundary scan architecture to at-speed test of inter-switch links in NOC for crosstalk faults. While we focus on the links, any non-modeled fault (inside or outside switches) that manifests itself as crosstalk on wires will also be detected by our method.

1.2. Prior work

Maximum aggressor fault (MAF) model [13] is one of the fault models proposed for crosstalk. Multiple Transaction (MT) model and its compacted set were proposed in [14] and [15], respectively. MAF model only considers cross-coupled capacitance, and intends to make the most serious crosstalk influence, while the MT model considers both cross-coupled capacitance and inductance. Consequently this model is more scientific. But the MT model needs a great deal of test pattern and its pattern redundancy is also serious.

Various approaches to analyzing the crosstalk are described in [16–19]. Interconnect design for GHz+ integrated circuits is discussed in [20]. The author observed that chips failed, when a specific test pattern (not included in the MA model) is applied to the wires, due to overall effect of coupling capacitances and mutual inductances. Several researchers have worked on test pattern generation for crosstalk. Authors in [21] proposed a test generation method for signal integrity faults on long interconnects. Order reduction algorithm is used to generate test patterns in order to decrease execution time [22]. Five modified boundary scan adaptive algorithms for Wire-OR (W-0) interconnect fault of PCB interconnects were also proposed in [23]. Test generation for capacitance and inductance induced noise and delay on interconnects is studied in [24–26].

There are a number of possible design and fabrication solutions to reduce crosstalk effects on interconnects [27–30], but none of them guarantees to resolve the issue perfectly.

Several methodologies were proposed for testing crosstalk faults on long interconnects between cores in SOC [31–33]. Authors in [34] also tested NOC communication infrastructure (included inter-switch links and switches) in a recursive manner. They reduced test application time with using uni/multicast mechanism to test data transmission. In [35] a Built in Self Test (BIST) strategy has also been presented for NOC communication infrastructure. This BIST is carried out as a go/no-go BIST operation at start-up, or on command. However, it has been proposed to use the NOC as a TAM during test of resources.

BIST-based test pattern generators for board level interconnects and delay testing were reported in [36] and [37], respectively. A test methodology targeting defects on bus structures using IDDT and boundary scan has been presented in [38]. This method is similar to boundary scan in terms of serial data transfer and, therefore, the extended Serial Interface Layer (SIL) architecture can be used for various test applications at the system level in general and in integrity test in particular.

IEEE 1149.4 mixed-signal test bus standard [39] was proposed to allow access to the analog pins of a mixed-signal device. In addition to the ability to test interconnects using digital patterns, 1149.4 includes the ability to measure actual passive components, such as resistors and capacitors. This standard cannot support high frequency phenomena such as crosstalk on interconnects. Ref. [40] proposes a method to simplify the development of a mixed-signal test standard by adding the analog interconnect test to 1149.1. IEEE 1149.6 provides a solution for testing AC-coupled interconnects between integrated circuits on printed circuit boards and systems [41]. Various issues on the extended JTAG architecture to test SOC interconnects for signal integrity are reported in [42], [43] and [31], which use MAF and MT fault models.

1.3. Contribution and paper organization

Due to time nature of crosstalk effects, they must be tested with functional speed of chip. So proving at-speed test with high speed Automatic Test Equipment (ATE) for GHz systems is expensive, because it needs testers with capability of GHz. On the other hand, test data transmission from an ATE to wires that are embedded in systems so deeply needs a TAM which occupies unacceptable area overhead. Compared to these techniques, BIST is a proper method for testing at-speed of crosstalk faults because it eliminates the need of expensive ATE.

Our main contribution is an at-speed test mechanism based on IEEE 1149.1 standard to test crosstalk faults on inter-switch links in communication infrastructure of NOC. Our method utilizing BIST technique and only one new instruction to test high frequency behaviors provides at-speed test for crosstalk faults on the links. Contrary to our approach, the standard is intended to consider coupling effects among the wires such as open and short circuit faults.

At-speed generating MVT model patterns is provided using extending conventional boundary scan cells on output port of switches (called BRBSC) receiving only one seed. MVT pattern set is much more capable of testing the capacitive and inductive couplings between wires. Test responses are also captured by extended receiving-end boundary scan cells (called RABSC) and are analyzed in order to detect the faults. Using one new instruction in IEEE 1149.1 architecture, at-speed test execution