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Analysis and design of a 1.0-V CMOS mixer based on variable load technique

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ABSTRACT

A CMOS active mixer based on variable load technique which can operate at 1.0 V supply voltage is proposed and its operation principle, noise and linearity analysis are presented. Different from the conventional Gilbert mixer based on RF current-commutating, the proposed mixer controls the load impedance according to the LO signal. It has only two stacked transistors at each branch which is suitable for low-voltage applications. The mixer was fabricated in 0.18-μm 1P6M CMOS process and measured in 2.4-GHz ISM band. With an input 2.440 GHz RF signal and a 2.442 GHz LO signal, the conversion gain is 5.3 dB, the input-referred third-order intercept points is 4.6 dBm, the input-referred 1 dB compression point is −7.4 dBm, and the single-sideband noise figure is 21.7 dB. Total DC current consumption is 3.5 mA.

1. Introduction

Highly integrated, low voltage and low power are the essential goals in integrated circuit design. These characteristics are especially critical in mobile wireless communication systems due to the limitation of battery capacity. With the reducing scale of CMOS technologies, the key problem of migration to advanced CMOS technologies comes from continual reduction in supply voltages, resulting in poor performance in analog and RF circuits [1,2]. Insufficient voltage headroom results in some circuit topologies unable to satisfy the required specifications or even unable to operate. Hence, research for low-voltage circuit topologies is important [1–7].

Mixer is the core component in both transmitter and receiver, it operates with low supply voltage and low power. The Gilbert-type mixer is the most mature mixer architecture widely used as the down-converter in CMOS superheterodyne receiver. In this type of mixer, the g_m stage are stacked on top of the current source tail, the switching pairs are stacked on top of the g_m stage, and finally, the load are placed on top of the switching transistors. Due to large number of stacked transistors at a low voltage supply and the voltage drops across the load resistors, the switching transistors and the transistors in the transconductor become critical, so this architecture cannot be used in CMOS advanced technologies which work with low supply voltage below 1 V [1,2].

To reduce the supply voltages, some folded mixer architectures have been investigated in [2,5], they can work well with 1.0 V supply voltage. However, as mentioned in [1], for the folded mixer in [2]: (1) The peak-to-peak amplitude of LO signal is lower than supply voltages. (2) The circuit cannot be easily biased, in spite of the fact that the linearity and especially *IIP3* performance of this circuit depends on proper biasing of transistor and switching section. (3) The switches are biased at non-zero drain current, which contributes more flicker noise to the output and increases the mixer's noise figure. The linearity of the folded mixer in [5] is very low. Moreover, it consumes too large DC current, and the noise figure will be large for low RF signal level.

A folded-cascode even harmonic mixer (FEHM) for low-voltage was investigated in [6]. It can operate in 0.9-V low voltage, but the frequency-doubling technique must be employed in the local oscillator (LO) stage to produce a LO double-frequency signal, and two LC-tanks have to be adopted to reduce the voltage headroom and select the LO double-frequency signal, which would enlarge the chip area. Moreover, to improve the linearity and avoid gain degradation, an off-chip resistor-turning network composed of two large resistors has been adopted between the output of the current reuse circuit and the input of the buffer, and the *IIP3* performance is strongly dependent on the value of the resistor-turning network and the DC bias voltage of RF stage and LO stage.

Another candidate for low-voltage application is the switched transconductor mixer [7], it utilizes switches connected to the supply voltage. The source of the g_m stage is switched to the ground and $V_{dd,sw}$ in each LO period, which will generate considerable switching noise. Moreover, as the $1/f$ noise of g_m stage is mixed up, and the mixer needs two DC supply voltages (i.e. V_{dd} and $V_{dd,sw}$).

In this work, a low-voltage CMOS down-conversion mixer controlling its variable load according to the LO signal to achieve

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mixing is proposed. It was implemented in 0.18-μm 1P6M CMOS process and measured in 2.4-GHz ISM band. We focus on the operation principle and measurement results of the mixer in [8], the noise and linearity analysis of this are focused on in this paper.

This paper is organized as follows: The proposed active variable load mixer core's operation principle and its conversion gain are presented in Section 2. In Section 3, the noise and linearity of the mixer are analyzed. The design process and the experimental results of the proposed mixer are shown and discussed in Section 4. Finally, Section 5 is the conclusion of this paper.

2. Operation principle of the proposed mixer

The single balanced version of the proposed mixer enhances suitability for low-voltage applications based on variable load technique instead of RF current commutating, as shown in Fig. 1(a). V_{B0} and V_B are DC bias voltage. Transistor M2 operating in triode region acts as the variable load. Its conductance $G_L(t)$ is controlled by the LO signal $v_{LO}(t)$, that is

$$G_L(t) = \beta_p(V_{DD} - V_B - v_{LO}(t) - |V_{THP}|), \tag{1}$$

where β_p is the transconductance parameter, V_{THP} is the threshold voltage of PMOS transistors. In this work, $G_L(t) = 0$ in the case of $V_{DD} - V_B - v_{LO}(t) - |V_{THP}| < 0$ for simplification. When $v_{LO}(t) = V_{LO}\sin \omega_{LO}t$, $G_L(t)$ can be expanded in a series of sinusoids:

$$G_L(t) = g_{L,0} + \sum_{n=1}^{\infty} g_{L,n} \sin(n\omega_{LO}t). \tag{2}$$

When $V_{LO} \le V_{DD} - V_B - |V_{THP}|$, $g_{L,0} = \beta_p(V_{DD} - V_B - |V_{THP}|)$, $g_{L,1} = -\beta_p V_{LO}$, and $g_{L,n} = 0$ for $n > 1$. On the other hand, the harmonic components $g_{L,n}$ $(n = 3,5,7,\ldots)$ generate when $V_{LO} > V_{DD} - V_B - |V_{THP}|$. In this case, $g_{L,0}$ and $g_{L,1}$ are given by

$$g_{L,0} = \beta_p V_{LO}\left[\left(\frac{1}{2} + \frac{\theta}{\pi}\right)\sin\theta + \frac{\cos\theta}{\pi}\right], \tag{3}$$

$$g_{L,1} = -\beta_p V_{LO}\left(\frac{1}{2} + \frac{\theta}{\pi} + \frac{\sin\theta\cos\theta}{\pi}\right), \tag{4}$$

where

$$\theta = \sin^{-1}\frac{V_{DD} - V_B - |V_{THP}|}{V_{LO}}. \tag{5}$$

Transistor M1 acts as the transconductance (g_m) stage, and operates in saturation region. To derive the down-conversion output voltage of the circuit, focusing on RF input and IF output frequencies, $v_{RF}(t)$ and $v_o(t)$ are expressed as

$$v_{RF}(t) = v_{rf}\exp(j\omega_{RF}t), \tag{6}$$

$$v_o(t) = v_{o,rf}\exp(j\omega_{RF}t) + v_{o,if}\exp(j(\omega_{RF} - \omega_{LO})t). \tag{7}$$

The relationship among v_{rf}, $v_{o,rf}$ and $v_{o,if}$ in Fig. 1(a) can be written as

$$\begin{aligned} &v_{o,rf}\exp(j\omega_{RF}t) + v_{o,if}\exp(j(\omega_{RF} - \omega_{LO})t) \\ &\quad = -Z_L(\omega_{RF})[g_{mN}v_{rf}\exp(j\omega_{RF}t) + g_{L,0}v_{o,rf}\exp(j\omega_{RF}t)] \\ &\qquad -Z_L(\omega_{RF} - \omega_{LO})[g_{L,0}v_{o,if}\exp(j(\omega_{RF} - \omega_{LO})t) \\ &\qquad +((jg_{L,1}/2)v_{o,rf}\exp(j(\omega_{RF} - \omega_{LO})t))], \end{aligned} \tag{8}$$

where g_{mN} is the transconductance of the NMOS M1. From this equation, $v_{o,rf}$ and $v_{o,if}$ are given by

$$v_{o,rf} = -\frac{g_{mN}Z_L(\omega_{RF})}{1 + g_{L,0}Z_L(\omega_{RF})}v_{rf}, \tag{9}$$

$$v_{o,if} = -\frac{j}{2}\frac{g_{L,1}Z_L(\omega_{RF} - \omega_{LO})}{1 + g_{L,0}Z_L(\omega_{RF} - \omega_{LO})}v_{o,rf}. \tag{10}$$

Thus, the voltage conversion gain (G_v) of the mixer is given by

$$G_v = \frac{v_{o,if}}{v_{rf}} = \frac{j}{2}\frac{g_{mN}Z_L(\omega_{RF})}{1 + g_{L,0}Z_L(\omega_{RF})} \times \frac{g_{L,1}Z_L(\omega_{RF} - \omega_{LO})}{1 + g_{L,0}Z_L(\omega_{RF} - \omega_{LO})}. \tag{11}$$

When $Z_L(\omega_{RF}) \gg 1/g_{L,0}$, $Z_L(\omega_{RF} - \omega_{LO}) \gg 1/g_{L,0}$, $|G_v|$ is $g_{mN}|g_{L,1}|/2g_{L,0}^2$. Fig. 1(b) shows dependence of the voltage conversion gain on LO amplitude V_{LO} in this case. In small LO amplitude region, the conversion gain increases proportionally to LO amplitude, which originates from $g_{L,1}$. With large LO amplitude, the conversion gain saturates and even decreases slightly due to increase in $g_{L,0}$. From these analytical results, to improve the voltage conversion gain, the β_p (i.e. W/L) of the PMOS should be decreased, and V_B and g_{mN} should be increased.

The mixer core proposed in Fig. 1(a) has some disadvantages. Firstly, it can be seen from Eqs. (9) and (10) that the RF feedthrough term exists in the output voltage, and it is larger than the mixing term. Secondly, the LO feedthrough will be found in the output if DC current of M1 is taken into account. To solve these disadvantages, the double balance structure is proposed as shown in Fig. 2. It is composed of four parts identical to Fig. 1(a), four resistors R are used

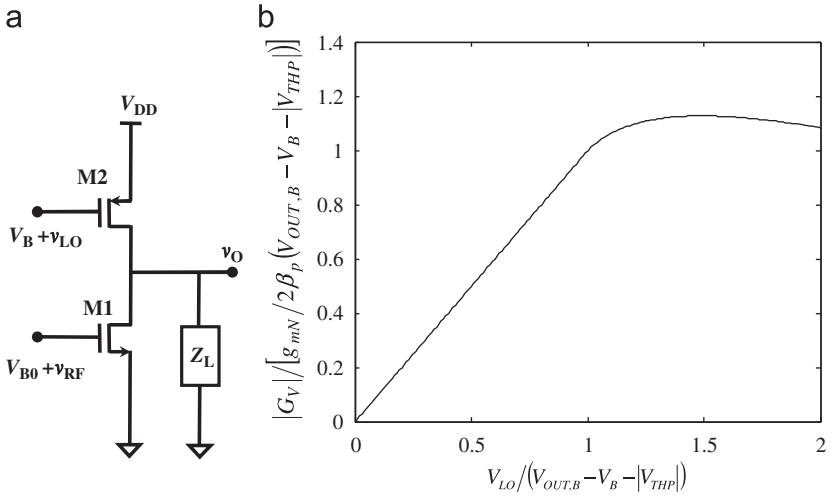

Fig. 1. The proposed mixer based on variable load technique. (a) Basic operation principle of the proposed single balanced mixer and (b) its voltage conversion gain (G_v) versus LO amplitude.