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Evaluation of the full operational cycle of a CMOS transfer-gated photodiode active pixel

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ABSTRACT

In this paper we evaluate the full operational cycle of the active-pixel circuit for CMOS image sensors in which four field-effect transistors are suitably combined with an ordinary photodiode; meaning a vertical p–n junction, as opposed to photogates, and with no custom pinned layer. Although this circuit topology itself is not novel, this evaluation intends to shine new light on the use of regular photodiodes. They became largely in disuse in four-transistor image chips under earlier process and design circumstances because the fourth transfer-gate FET did not hold a constant signal long enough and not for a fixed time. Our aim is to investigate the full underlying operational regimen of the transfer gate to propose that a regular photodiode might again be a choice to consider in the four-transistor pixel configuration, not only in conventional imaging but also in dedicated optical applications. The use of an ordinary p–n junction photodiode is advantageous as it offers full compatibility with even elementary mainstream CMOS processes. This investigation resorts to experiments and models both with fabricated integrated pixels and with a macro-pixel circuit implementation.

1. Introduction

Image sensors are ubiquitous in modern society and are based on semiconductor technologies led by silicon. In that realm, either standard or tailored CMOS processes enable the integration of photodetection capability with reliable electronic functionality on a single chip. Most CMOS image sensors are focal-plane arrays of active pixels [1], referred to as Active-Pixel Sensors (APS). In APS, the photogenerated current or charge of an exposed sensitive element is translated into an output pixel voltage by means of a simple source-follower circuit, i.e. a buffer MOSFET. This circuit electrically decouples the photosensitive element from the signal bus. A number of active-pixel circuit architectures have been reported where the number, type and internal connection of transistors vary considerably [2]. The conventional APS approach involves only three transistors: reset (Rst), select (Read) and Buffer transistors; and a p–n junction photodiode as the sense element [3]. In this 3T APS, during a specified integration time, the internal junction capacitance, previously charged to a reference voltage by means of the Rst transistor, is discharged by a photogenerated current. By monitoring the Buffer output voltage during a preset integration time, one infers the voltage drop across the junction capacitor, and therefore the magnitude of the photocurrent. The Read transistor enables the output of a particular pixel to the signal bus.

While exposed to light, or even due to reverse dark current, the photodiode continuously acts on the discharge of the internal capacitance, which is only counterbalanced by maintaining the Rst transistor on. Therefore, as pixels on an array are usually reset simultaneously and read out sequentially (rolling shutter), a uniformly illuminated imaging chip outputs an image with some degree of inhomogeneity. In the strictest sense, neither true random access, i.e. temporal and spatial, nor an in-pixel global electronic shutter can be realized to 3T pixels across a matrix. Hence, photodiodes have also been attempted with the four-transistor (4T) APS, where an additional transistor, often termed *transfer gate* (Tx) or shutter-control transistor, operates the electrical connection between the photodiode (PD) cathode and the sense node in a sample-and-hold fashion [4]. The fourth transistor, termed transfer gate, bridges the photodiode to the remaining pixel circuit and disconnects the photodiode, after the photon integration time, to maintain the signal constant at the output. This relaxes the readout time and enables multiple non-destructive read-outs. The transfer gate should confer a sample-and-hold feature to the pixel. From the transistor regimen stand point and provided the noise floor of the technology is low enough, this might be especially suitable for very low photocurrents, prevailing in

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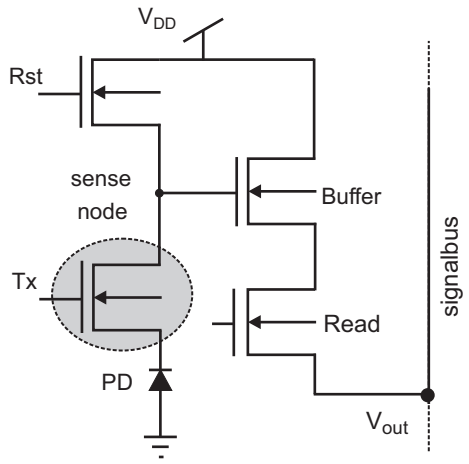

Fig. 1. Basic schematics of the conventional circuit for the 4T photodiode active pixel, where the Tx FET has been included between the ordinary photodiode (PD) and the sense node.

low-light conditions or in high-resolution submicron CMOS imagers, where photons per pixel decrease. Fig. 1 shows the circuit topology with the conventional reset transistor (Rst), read transistor (Read) and source follower (Buffer), plus a fourth NMOS Tx transistor [4], introduced between the sense node and the photodiode that was to be abandoned and replaced by charge accumulation and/or presumably less noisy alternatives.

Transistor Tx can be useful to enable signal averaging through multiple readings on the same pixel and to permit true correlated double sampling (CDS) for the reduction of fixed-pattern and reset noise [5]. However, especially in the consumer imager scenario, the 4T *regular p–n junction* photodiode APS appears to have faded to oblivion. This might have been premature, though, supposedly under the argument that, for constant exposure, the photodiode introduced instability to the transfer-gate regime and rendered the pixel voltage signal (V_{out}) unreliable, as the signal was not maintained constant at the sense node, often referred to as floating diffusion. This unsteadiness can indeed occur, but mostly for relatively large photocurrents. In general, the employment of the additional Tx transistor results in an increase in the pixel area and of the intrinsic $1/f$ noise, besides the undesirable transient channel–charge redistribution [6].

Yet, the 4T topology has not ceased altogether to be employed, but was instead adopted as a commercial solution relying on charge accumulation, rather than on current flow, by replacing the photodiode by either a photogate, basically a MOS capacitor, or a *pinned* photodiode, i.e. a specific photodiode topology with a specially tailored surface layer pinned to the substrate [7]. Nonetheless, despite several merits, the first alternative is affected by reduced blue sensitivity and requires either overlapping poly-Si layers or reliable transfer diffusions. The second structure, a pinned photodiode, is also inherited from the CCD technology and works based on charge accumulation in the depletion layer rather than on direct photocurrent generation. This structure features low dark-current noise, achieved by the isolation of surface energy states, but demands additional photodiode area and biasing, and dense shallow boron implants, specially designed on an n-layer. These optimized shallow implants are usually not directly available in standard CMOS processes and are often replaced by adapted surrogates (e.g. STI or LOCOS p^+ stoppers) [8]. The pinned photodiode configuration also exhibits a limited charge-storage capacity in the depletion layer and is known to introduce image lag due to incomplete pixel reset and requires an optimized transfer gate [9,10].

In this paper we revisit the ordinary photodiode, as a photocurrent source, in a 4T APS configuration with the transfer gate as in Fig. 1. We investigate the operational regimen of the transfer gate and propose that under certain conditions, in tune with the reduction trends in both CMOS feature size and pixel size, it might again be a choice to consider, especially for very low photocurrents. When Tx is connected between the photodiode and the sense node it is meant to really switch on and off the photodiode from the circuit, leaving a intrinsically larger parasitic capacitance to hold the signal composed by the sense node/Tx-drain/Reset-drain capacitance in association with the sense node/Buffer-gate-source capacitance. An alternative 4T photodiode APS connects Tx between the sense node and the Buffer, resulting in a lower accumulation capacitance, resulting in sooner saturation of the pixel, therefore suitable for shorter integration periods. This choice does not present a drop to negative voltage values across the photodiode and is appropriate when a synchronous shutter is demanded especially for high-frame-rate high-density imagers in snap-shot mode.

Although very important for a full assessment prior to a new design, dynamic range and noise analysis is not the focus of this work and should be pursued in a follow-up paper. One must observe, however, that although dark-current shot noise is known to be larger in ordinary photodiodes than in pinned photodiodes, the dynamic range is at least comparable. This follows because on the upper limit the pinned-photodiode charge storage is restricted, whereas the saturation currents in regular photodiodes are rather large. To guide a sensible decision, the bottom limit plays a crucial role and a pixel designer must verify the photocurrent levels to be practiced in a given application and contrast the expected photodetector dark-current noise with the noise floor in the chosen CMOS technology [11].

This study is conducted by means of models and experiments both with a fabricated CMOS pixel and with a macro-pixel implementation. The physical operation of a generic transfer-gated APS with a photodiode will be systematically investigated, revealing that parasitic elements play an important role in its understanding. We also experimentally verified the appearance of negative voltage levels across the photodiode terminals when integration time is long enough, a fact indicated by simulations, but often neglected in practical APS structures. This behavior proves important in explaining some of the underlying physical phenomena ruling the operational regime of the transfer-gate transistor. We believe the voltage drop to negative values is present in every sensor using a transfer-gate FET between a *regular* photodiode and the sense node, regardless the feature-size of the technology, as it results mainly from the reverse (re)charging of the photodiode junction capacitance, and from its intrinsic features, rather than from the FET characteristics. The output voltage after the source follower in APS structures will always be positive, despite the voltage being negative across the photodiode. The pixel output voltage is often the one reported in the literature as it is the figure of interest for the evaluation of image-sensor performance. Nevertheless, acknowledgment that there is a situation in which the photodiode voltage becomes negative fosters the understanding of how long the Tx can sustain a regimen in which the output voltage is held constant. Photogate and *pinned* photodiodes behave differently as they rely on direct charge reading rather than on the photocurrent generated by *ordinary* photodiodes as reported in this paper.

2. Transfer-gated photodiode structure

The circuit for the 4T photodiode APS analyzed henceforth is shown in Fig. 2. The photodiode model includes a current source