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Test data compression using interval broadcast scan for embedded cores

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ABSTRACT

The paper proposes a new test data compression scheme for testing embedded cores with multiple scan chains. The new compression scheme allows broadcasting identical test data to several scan chains whenever the cells in the same depth are compatible for the current application test pattern. Thus, it efficiently utilizes the compatibility of the scan cells among the scan chain segments, increases test data run in broadcast mode and reduces test data volume and test application time effectively. It does not need complex compressing algorithm and costly hardware. Experimental results demonstrate the efficiency and versatility of the proposed method.

1. Introduction

With both test data volume and circuit size growing and feature size shrinking, rapidly growing test costs are severely challenging the applicability of scan-based testing. Test data compression addresses this problem by reducing the test data volume without affecting the overall system performance.

Different compression techniques have been proposed over the years to reduce the test data volume. Some of them are based on coding scheme, such as run length coding [1], Golomb coding [2], FDR coding [3], selective Huffman coding [4], run length Huffman coding [5], 9-coded technique [6], block merging [7], Multi-Dimensional pattern Run-length Compression (MDPRC) [8], optimal-selective Huffman coding [9], etc. These coding schemes all mainly target on the given test sets for a single scan chain.

Recently, some methods in practice assume a 1-to-n scan configuration to reduce test data volume, in which the number of internal scan chains is n times the number of external scan I/O ports [10]. The greatest challenge in scan test cost reduction with a 1-to-n scan configuration is how to bridge the gap between external scan ports and internal scan chains. Two major types of solution for solving this challenge are those based on linear decompression scan and those based on broadcast scan. Linear decompression-based schemes encode for the test cubes generated by ATPG for a 1-to-n scan configuration circuit, which contain lots of don't care bits through solving a set of linear equations. Embedded deterministic test (EDT) [11] belongs to this type; the method requires at least an additional clock to control the sequential logic operation. Reseeding techniques, which compute a seed (an initial state) for each test cubes [12–15] for single scan chains and some schemes, which encode for test slices for multiple scan chains [16–18] are both linear decompression-based compression methods, and the compression ratios are related to the number of scan chains for multiple scan chains methods. Broadcast scan-based schemes use an external scan input port to drive multiple internal scan chain inputs through combinational logic only. Such as Virtual scan [10], which uses XOR gates or multiplexers as decompression. Illinois scan (ILS) [19,20], which proposes direct external and internal connections.

There are also some other data compression works based on scan chains reconfiguration, low power testing or test set compatible. An incremental algorithm for ILS test generation was presented in paper [20]. Scan chain reconfigurable technique was proposed for ILS [20,21]. Low power ILS(s) techniques were presented in papers [23,24]. A low power compression scheme is presented in paper [25] in test compression environment. The compression methods presented in papers [26,27] are all based on the compatibility of the test set, and paper [28] presented a scan partition technique to make the test set more regular.

The paper presents a test data compression scheme for intellectual property (IP) cores with multiple scan chains. For this kind of IP cores, no reconfigurations or modification could be done on them, and none of the prior compression works mainly target on them to the best of our knowledge. The proposed method allows broadcast test data to several scan chains whenever the cells in the same depth are compatible for the current application test pattern. So, it enhances broadcast mode's test

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application data, and reduces test data volume and test application time accordingly without harming the fault coverage. The hardware overhead is very small. We assume a pre-determined order of scan cells, and determine group configurations without constraints on the number of groups. The main contributions of the paper are as follows:

1. Primarily introduces interval broadcast data to many scan chains to reduce test data volume and test application time for embedded cores.
2. Proposes the new 1-to-*n* scan configuration scheme for multiple scan chains IP cores with low overhead.
3. Primarily uses interval broadcast scan to make single scan chain compression schemes adapt to compress multiple scan chains IP cores.
4. Gives simple analysis for test data and test application reduction and a simple discussion for the proposed scheme.

The rest of the paper is organized as follows. The motivation is given in Section 2. Section 3 presents the proposed interval broadcast scheme. The proposed scheme work with other single scan chain methods to make them adapt to compress multiple scan chains IP cores is given in Section 4. A simple discussion is shown in Section 5. Experimental results appear in Section 6. The last section is devoted to a simple conclusion.

2. Motivation

To reduce scan-shift operations for single full scan circuits, the multiple scan chains architecture was proposed [29]. As shown in Fig. 1, the multiple scan technique divides a single scan chain into a number of shorter scan chain segments and thus reduces the time needed to shift input/output vectors. In the multiple scan approach, the test time reduction is achieved using more test pins, while the test data volume is unchanged [30]. Many test data compression schemes have been proposed to reduce the test data volume and the tester channel requirements. Fig. 2 shows the compression architecture with a 1-to-*n* scan configuration: a compressed vector is loaded from the tester into the decompressor, which feeds the decompressed vector into the scan chains. The amount of output response can also be reduced by output compression techniques. These works are all design for testing at an early design stage. However, for an IP core with multiple scan chains, we could not redesign it for compression.

Most coding-based compressing schemes [1–9] target on IP cores with single scan chains. When applied on IP cores with multiple scan chains, most of these methods use an *n*-bit shifter (where *n* is the number of scan chains) to input test data serially, as shown in Fig. 3. The shifter shifts the data from signal of D-out to the scan chains and an additional counter_*n* to control shifting

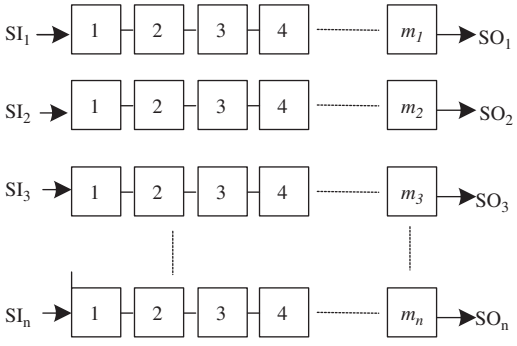

Fig. 1. Multiple scan chains architecture.

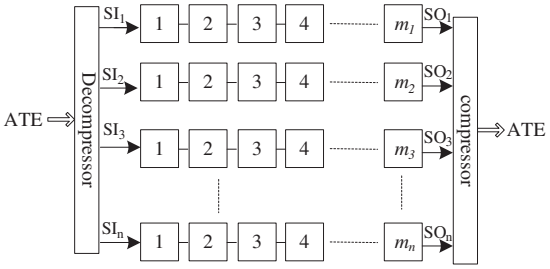

Fig. 2. Multiple scan chains architecture with input/output compression.

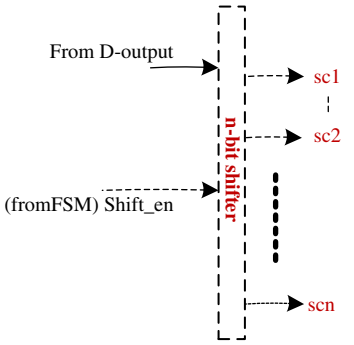

Fig. 3. *n*-Bit shifter for decompressing multiple scan chains for coding-based compression schemes.

n bits into *n*-bit shifter. When counter_*n* reaches 0 it notifies the *n*-bit shifter to load its content into the scan chains *sc*1 to *scn*. However, in this case we cannot exploit the benefits stemming from the existence of multiple scan chains with respect to the test application time. To solve this problem, the interval broadcast scan is proposed, which is the motivation of the paper.

3. Proposal

To reduce test pins, test data volume and test application time for IP cores with multiple scan chains (as shown in Fig. 1), the proposed scheme allows interval broadcast test data to multiple scan chains using only one test pin as 1-to-*n* compression configuration.

An architecture example of the proposal is given in Fig. 4. The architecture has *n* scan segments with *m* scan cells each. The hardware required includes *multiplexers* (*MUXs*) for each scan chain segment and a *shift register*. Scan cells in the same depth share same test data if they receive compatible test logic value. Otherwise, the incompatible data will be shifted serially through the *shift register*. The *MUXs* are used to choose data from scan-in (*SI*) and the register. If the *MUX-select signal* is high, *SI* feeds all the scan chains with same data. Otherwise, the *shift register* receives the new scan-in data from *SI*, and the *shift-enable* is inactive to prevent all scan chain segments shifting, the *module-n counter*(*n* is the number of scan segments) controls the operation of shifting data to the shift register. The signal of shift-enable is enabled when the *mode-m counter* is zero. The output of each scan chain is connected to a multiple input signature analyzer (MISR). The *MUX-select signals* are decided by the compatible of the corresponding same depth test data, and the corresponding MUX-select signals must be stored.

A test vector operating in interval broadcast mode is given in Fig. 5. The architecture has 5 scan segments with 9 scan cells each. A vector is applied to the architecture and has compatible data in all depths except depth 2 and depth 7. Thus, the data of d1, d3, d4, d5, d6, d8 and a9 are broadcasted, while the data of