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A prognostic method for the embedded failure monitoring of solder interconnections with 1149.4 test bus architecture

Juha Voutilainen[a,*], Jussi Putaala[b], Markku Moilanen[a], Heli Jantunen[b]

[a] *Optoelectronics and Measurement Techniques Laboratory, University of Oulu, Finland*

[b] *Microelectronics and Materials Physics Laboratories and EMPART Research Group of Infotech Oulu, University of Oulu, Finland*

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Abstract

This paper describes the feasibility of accurate low frequency measurements in predicting the breakdown of modern lead free ball grid array (BGA) interconnections. In these measurements, performed partly with 1149.4 analogue boundary scan, ceramic BGA modules measuring 15×15 mm in width, with 9×9 ball matrixes, were attached on an FR-4 printed wiring board (PWB) and thermally cycled over a temperature range of -40 to $+125\,°C$. The condition of corner interconnections was monitored using the developed measurement methods and construction. *In-situ* measurements were performed with a datalogger during temperature cycling, accompanied with 1149.4 mixed-signal test bus measurements of corner interconnections performed between cycling intervals. In addition, the measurements were complemented by scanning acoustic microscopy and, X-ray. Monitoring corner interconnections by a simple, low-frequency voltage measurement method with embedded test constructions gives an early warning indication well before the electrical interconnection failures. Of two studied interconnection compositions, the ones with plastic core solder balls (PCSB) proved to be more reliable than the ones with 90/10 PbSn balls.

Keywords: Proactive diagnostics; 1149.4 Analogue boundary scan; Thermal cycling; Reliability; Solder joint

1. Introduction

Significant aspects in the engineering of modern electronics are the design for testing and the increasing reliability demands placed on electronics products. Factors such as package size reduction, diminishing interconnection height and other similar trends often challenge the testability and compromise the reliability of electronic products. In addition, new EU legislation, "the restriction of certain hazardous substances in electrical and electronic equipment" (RoHS), prohibits the use of lead, with the exemption that high melting temperature solders (over 85% of lead) are still allowed [1]. This is yet another aspect that will affect the reliability of future electronic products.

When considering a typical electronics assembly, for example a ceramic ball grid array (BGA) package attached on an FR-4 printed circuit board (PCB), the weakest links in terms of reliability are usually its interconnections, which serve as thermal, mechanical and electrical connections. These interconnections must withstand a diversity of loads, including mechanical vibration, electro- and metal migration and—possibly foremost in electronics products—variation in temperature. This temperature variation can be produced either by internal (device on/off operation) or external (outside temperature changes) factors or, more commonly, by both together. The consequently occurring stresses arise mainly from different thermal expansion coefficients of the used materials, accompanied with varying thermal gradients in different parts of the product.

The thermal expansion coefficients (CTE) of ceramic and PCB materials are typically in the range of 5–8 and 14–16 ppm/K, respectively. In addition, the different CTEs of metals used in the interconnections add up to the problem, making the thermal mismatch even more noticeable.

Past and present self-test systems are based mainly on "digital" fault detection. First, localization of the

*Corresponding author. Tel.: +358 8 553 7682; fax: +358 8 553 2774.
E-mail address: vouti@ee.oulu.fi (J. Voutilainen).

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component is performed, followed by a functional test to assure its proper operation—and thereby that of the whole device. This is a fairly convenient way to proceed, especially in production testing, but alternative means are required to improve the reliability of prediction methods in field use and to allow the realisation of embedded test structures capable of predicting the product's maintenance needs.

In the laboratory environment, interconnection monitoring during thermal cycling tests (TCT) is typically conducted by tracking resistance changes in interconnections connected in daisy chains. A chain can be interpreted to be broken, for example, when its initial resistance value is doubled [2]. However, presently used methods are not very accurate in detecting wear out, in other words, the correlation between electrical and mechanical deterioration is somewhat deficient.

There is an impending need to improve the measurement accuracy of new package structures. In this way, the predictability of solder joint failures can be improved by increasing the prognostic distance (the time difference between final breakdown and first evidence of forthcoming failure) relative to daisy chain measurements. This allows early warning signs of failure to be obtained before an actual electrical breakdown [3].

The most practical way of performing *in-situ* monitoring of critical parameters in field use, is the utilization of embedded measurement techniques with the early warning capability.

Converting the idea of prognostic *in-field* and *in-use* monitoring to novel BGA packages allows the introduction of embedded test methods (IEEE 1149.4 Mixed-Signal Test Bus Architecture) and inbuilt test structures [4]. The prognostic monitoring concept is enabled by the use of corner balls as monitoring targets and then routing test signals with these interconnects. For example, using the corner balls of BGA structures as monitoring targets and the middle ball as reference in a bridge configuration, we achieve enough measurement accuracy for detecting the first evidence of a final breakdown in advance.

The implementation of inbuilt or embedded test structures for prognostic monitoring or reliability prediction with embedded/discrete components in the device can be considered a challenging task. By using embedded test methods, such as the IEEE 1149.4 Mixed-Signal Test Bus Standard, prognostic monitoring can be shifted from external measurements to *on-board* measurements, which is the current main trend in testing techniques.

This paper utilized interconnection failure monitoring based on DC bridge voltage measurements. One of the main goals was to investigate the usability of the 1149.4 analogue boundary scan in performing these measurements.

Two types of RoHS-compatible BGA interconnection compositions were used; one with 90/10 PbSn balls and the other with plastic core solder balls (PCSB) [5]. Ceramic packages with these types of interconnection in a 9×9 array were attached on an FR-4 PWB and thermally cycled. Weibull reliability figures of the interconnection structures will be presented.

The results of this research prove that (1) a cost-effective interconnection degradation monitoring tool based on the 1149.4 analogue boundary scan is a reasonable solution for use in future electronics and (2) the use of PCSB in interconnections increase their reliability when compared to ordinary 90/10 PbSn BGA balls.

2. Theory

While emphasizing the importance of data analysis methods, this chapter briefly presents the underlying measurement theory with the necessary equations. In addition, a definition of slope matrix is given with an explanation of failure criteria in BGA solder joint monitoring measurements.

2.1. Calculation of BGA prognostic ball resistances

In agreement with the measurement bridge theory, the measurement principle takes into account the contribution of temperature changes caused by cycling. From the differential off-balance voltage V_{OB} arising from bridge instability and the total voltage over the measurement bridge V_{B}, we can write the total impedance of the bridge as

$$R_{\mathrm{TOT}} = \frac{(B_1 + B_2)(R_1 + R_2)}{(B_1 + B_2) + (R_1 + R_2)}. \tag{1}$$

Then, using Kirchoff's voltage and current laws, the bridge theory gives us the bridge instability condition ($V_{\mathrm{OB}} \neq 0$):

$$V_{\mathrm{OB}} = V_{\mathrm{OB(H)}} - V_{\mathrm{OB(L)}} = V_{\mathrm{B}}\left[\frac{R_1}{R_1 + R_2} - \frac{B_2}{B_1 + B_2}\right] \tag{2}$$

where R_1, R_2, B_1 and B_2 are the resistors forming the measurement bridge. Voltages $V_{\mathrm{OB(H)}}$ and $V_{\mathrm{OB(L)}}$ are depicted in Fig. 1. It is assumed that no current flows trough the measurement ball B_{m}, since the measurement equipment has a large input impedance. Now, if we take

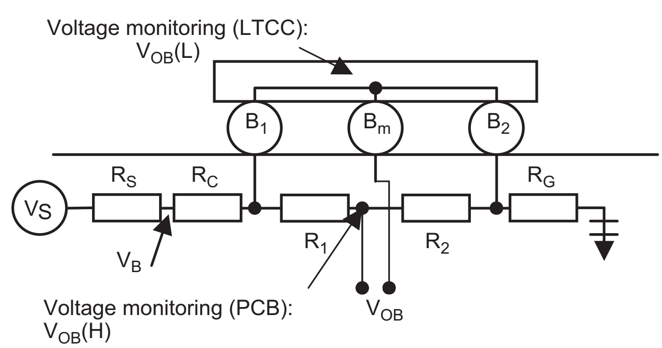

Fig. 1. Electrical schematics of single monitored corner balls.