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Review Article

Making lithography work for the 7-nm node and beyond in overlay accuracy, resolution, defect, and cost

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ABSTRACT

Overlay accuracy, resolution, defect, and cost are identified as the major challenges to extend lithography to the 7-nm node and beyond. Overlay accuracy is of the highest concern because it is not scalable with a more powerful lens or a shorter wavelength. It is dictated by mechanical precision and the ability to measure overlay errors. It also depends on non-litho fabrication techniques. We propose five approaches in wafer processing and four approaches in mask making to improve overlay accuracy. We also point out other means to pursue instead of squeezing overlay accuracy by brute force. Resolution and the corresponding process window are compared among ArF water immersion lithography, EUV lithography, and multiple e-beam direct write lithography. The limitation by resists may become the ultimate showstopper in resolution. At the advance of each node, the threshold of defect size is automatically tightened for defects on masks and on wafers. Mask defects can be in the absorber and the blank. Defects can come from contamination or cleaning. Even with maskless e-beam lithography, the in situ programmable mask can be contaminated. Defects can also be generated during wafer exposure, wafer processing, and non-litho processing. Solutions are provided and their practicality discussed. Lithography cost to produce single-digit nanometer features can be the decisive showstopper. We show several cost scenarios using manufacturing considerations and discuss cost effectiveness.

1. Introduction

Lithography has been a faithful driver of Moore's law to enable doubling of circuit density since the minimum feature size (MFS) was in the 5-μm regime. After a brief period of proximity printing, the circuit patterns have always been imaged by projection optics. Decades later, the imaging wavelength evolved from visible to 193 nm; the numerical aperture of the imaging lens, from 0.18 to 1.35; resolution enhancement techniques facilitate printing from $k_1 = (W/\lambda)$ NA = 0.8 to reach $k_1 = 0.3$. Multiple patterning using more than one exposure, each followed by one etching for a given circuit layer, can further push k_1 much lower, at the expense of cost and process complexity. The industry needs to go to single-digit nanometer MFS in the foreseeable future. What are the challenges to overcome? Will lithography continue to be a faithful workhorse?

Table 1 shows a proposed specification of the 7-nm and the 5-nm nodes in terms of half pitch (HP), overlay accuracy for single machine overlay (SMO) and mixed machine overlay (MMO), defect, and cost. The HP follows a 70% reduction per node as expected of Moore's law. The overlay accuracy is about 13.5% of HP. Less than one defect is required to maintain an acceptable yield, especially as the number of masks increases significantly from node to node. Cost of each die on the wafer has to be kept below that of the last node to make it worthwhile advancing the node. This is the spirit of Moore's law.

Fig. 1 shows the progression of lithography schemes from g-line steppers to immersion scanners. The perished 157-nm scanner, pending extreme UV (EUV) scanner, and multiple-electron-beam direct write (MEB DW) tools are included. The resolution = wavelength line is drawn across all wavelengths. Initially, the HP from optical lithography was larger than wavelength. By the time of ArF wavelength, all half pitches were smaller than wavelength. Only with EUV, is above-wavelength resolution again possible but not for long. E-beam resolution is always larger than wavelength for generations to come at even 5 keV, as drawn. No matter larger or smaller than wavelength, resolution has always been improved successfully for each advancing node, and the required overlay accuracy has always followed resolution. However, this is no longer true for single-digit nanometer nodes.

Overlay accuracy is of the highest concern to push the IC circuits to the 7-nm node and beyond, because overlay accuracy is

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Table 1
Proposed specification of the 7-nm and 5-nm nodes.

7 nm node			5 nm node		
Half pitch	15 nm		Half pitch	11 nm	
Overlay accuracy	SMO	1.5 nm	Overlay accuracy	SMO	1 nm
	MMO	2 nm		MMO	1.5 nm
Defects	<1 per layer		Defects	<1 per layer	
Cost	<1.15–1.4 of last node		Cost	<1.15–1.4 of last node	

not scalable with a more powerful lens or a shorter wavelength. It is dictated by mechanical precision and the ability to measure overlay errors. It also depends on other non-litho fabrication techniques.

Resolution is the second concern for advancing single-digit nanometer nodes. Multiple patterning can handle pitches below the limit of a given imaging system but cost, cycle time, indirect alignment between the multiple patterned layers, and process complexity are issues. EUV lithography (EUVL) reduces the imaging wavelength by more than an order of magnitude to improve resolution without multiple patterning. However, because of reflective optics and lower surface precision with respect to wavelength, the NA of EUV systems cannot be as high as that of refractive ArF immersion lithography, DOF consideration also limits the NA in EUVL. EUV double patterning may be needed for some very critical layers in the 7-nm node and even more layers for nodes beyond 7 nm. E-beam imaging can provide high resolution and large DOF. But, even with high resolution in the aerial image, the resist is becoming a limiting factor.

Similar to overlay accuracy, the size of defects has to scale but it is becoming more and more difficult to do so. Also, defects cannot be improved with better resolution. Actually, better resolution makes more defects printable.

Last but not least, cost has to be considered. If cost is unlimited, the product easily becomes unaffordable, making it unnecessary to improve overlay accuracy, resolution, and defect density.

We now consider overlay accuracy, resolution, defects, and cost in detail.

2. Overlay accuracy

Overlay accuracy can be affected by non-lithographic processes. For example, a warped wafer due to high-temperature processing induces nanometer-level overlay errors, similar with wafer backside contamination. Multiple patterning reduces overlay accuracy due to indirect alignment between the multiple patterning steps. Mixing single and multiple patternings does not alleviate the problem. Only when single patterning is used through all critical layers, can one eliminate indirect alignment errors. We propose five approaches in wafer processing and four approaches in mask making to improve overlay accuracy. We also point out other means to pursue instead of squeezing overlay accuracy by brute force.

2.1. Overlay errors in multiple patterning

Double patterning uses several exposures and corresponding processing steps consisting of resist coatings, baking, developing, cleaning, etching, etc., to delineate the pattern of a semiconductor layer. This way there is no memory carried over from each masking step, enabling pitch splitting and clean cutting. The cost is more than just multiples of the exposure cost, because from the 2nd pattern transfer and on, the patterning transfer cost contributes to lithography cost.

The split patterns, employed in the multiple-patterning scheme, have to align to each other. In turn, they have to align to the multiple patterns in the previous circuit layer and to be aligned by the next circuit layer. Therefore, 2nd order and higher orders of indirect alignments are inevitable.

Fig. 2 shows the situation of a 2-photo 2-etch (2P2E) circuit layer aligned to a 3P3E circuit layer that was aligned to a 2P2E circuit layer. Within the 2P2E circuit layer at the bottom, the two patterns are aligned to each other directly. When the 3P3E layer overlays on the 2P2E layer, there are inevitably four 2nd-order alignments. Let us set the direct overlay accuracy at 1.5%. The 2nd order overlay accuracy is now 2.1% which is the direct overlay accuracy multiplied by *sqrt*2. Adding the 2P2E layer on top of the 3P3E layer as shown, produces one 2nd order alignment and four 3rd order alignments. The overlay accuracy at this layer can be as bad as 3%.

When a 1P1E circuit layer overlays to the previous configuration as shown in Fig. 3, there is still a contribution of 3rd order overlay accuracy. The only way to avoid the indirect overlay errors is to use 1P1E for all layers. Note that if the overlay tree is not optimized, the situation can be much worse, leading to 6th order overlay error as shown in Fig. 4.

2.2. Overlay error induced by wafer warping

A wafer that goes through high-temperature processes or film deposition can be warped, either due to stress release of

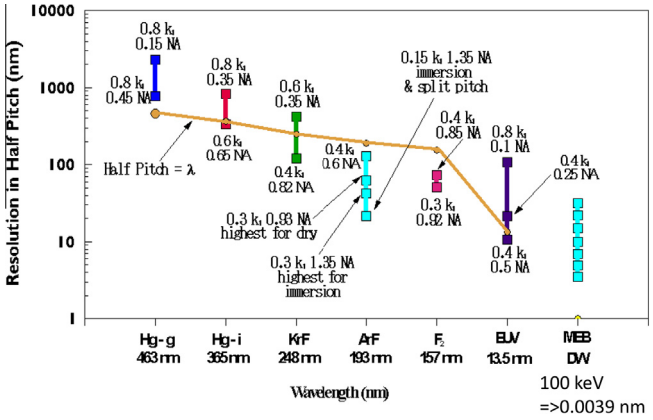

Fig. 1. Progression of lithography schemes.

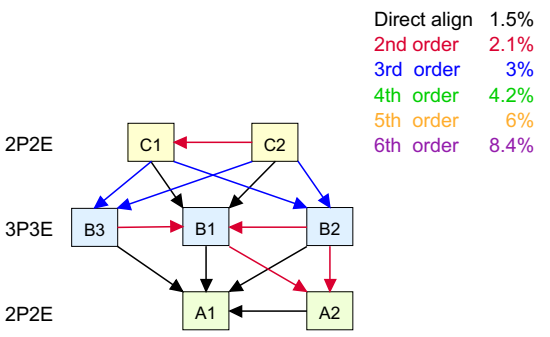

Fig. 2. Overlay tree of 2P2E aligned to 3P3E on 2P2E.