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Step-by-step growth of an epitaxial $Si_4O_5N_3$ single layer on SiC(0001) in ultrahigh vacuum

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ABSTRACT

An epitaxial single $Si_4O_5N_3$ layer was formed on a SiC(0001) surface using a step-by-step growth method in an ultrahigh vacuum condition. First, a silicon adsorbed SiC(0001) surface was prepared. The surface was then exposed to NO gas at 950 °C in order to form a Si_2ON_3 layer. Silicon was deposited on this surface and annealed to adjust the amount of adsorbed Si atoms. Finally, the surface was oxidized at 800 °C. The formation of a $Si_4O_5N_3$ layer was confirmed by low-energy electron diffraction analysis, Auger electron spectroscopy, and scanning tunneling microscopy. Using this procedure, we were able to suppress the growth of graphite-like clusters on the surface, although silicate-like clusters still remained.

1. Introduction

Surface and interface modification of silicon carbide (SiC) is very important to the further improvement of its intrinsic properties. SiC's wide band gap and high dielectric strength and thermal conductivity are useful in the development of energy-saving power devices as well as in device miniaturization [1]. To achieve optimal performance, the characterization of surfaces and interfaces is vital. Because silica layers can be grown on SiC substrates, practical applications of Schottky barrier diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) have been successful. Nevertheless, the interface between the SiC substrate and silica layer has a high interface state density [2,3], which can significantly weaken electronic features [4–6]. Therefore, it is necessary to find smooth, abrupt, robust, and dangling-bond- and contamination-free layers in order to develop perfect interfaces on the SiC substrate.

There are four determined $(\sqrt{3} \times \sqrt{3})R30°$ structures on the 6H- or 4H- SiC(0001) surface. These are: (i) a simple adatom structure of one silicon atom on the T_4 site of the SiC bilayer in the unit cell [7,8]; (ii) a single silicate layer with lateral Si-O-Si networks and vertical Si-O-Si bridges toward the SiC(0001) substrate with a chemical composition of Si_2O_5 [9,10]; (iii) a single silicon-nitride layer with an oxygen cap having a Si_2ON_3 composition [11]; and (iv) a hetero-double-layer structure with a single silicate layer and a single silicon-nitride layer connected by vertical Si-O-Si bridge bonds. The latter, which has the composition of $Si_4O_5N_3$ [12], is our target structure for this study. Structural models for the (i), (iii), and (iv) surfaces above are shown in Fig. 1(a), (b), and (c), respectively. The Si_2O_3 and $Si_4O_5N_3$ layers have the same honeycomb-like topmost silica structure, which has been also observed on Mo(112) surfaces [13]. In addition, similar bilayer-silica, called silicatene, have been obtained on Ru(0001) surfaces [14,15]. These are very stable because the topmost layer has no dangling bond; correspondingly, they are robust even under exposure to air. Such robustness is very important for use in many applications.

Epitaxial growth of a silica layer (Si_2O_5) on SiC(0001) using H_2 etching has been reported [9,10]. This method shows abrupt termination of the SiC(0001) substrate with a well-ordered single-layer silica of $(\sqrt{3} \times \sqrt{3})R30°$ unit, as in structure (ii) described above. However, because there is one intrinsic dangling bond in the unit cell, interface states are inevitable. On the contrary, in structure (iv) the silicon oxynitride layer ($Si_4O_5N_3$) on SiC(0001) is not only abrupt but also has no intrinsic dangling bond in the unit cell, and it exhibits a substantial band gap of 9 eV at its surface [12,16]. Such $Si_4O_5N_3$ layers are obtained by H_2 etching followed by N_2 treatment at 1360 °C at atmospheric pressure. Because the numbers of Si and C atoms are not controllable in this process, it is difficult to minimize residual Si and C atoms and their corresponding oxides [17]. These residual materials make interface states just above the $Si_4O_5N_3$ layer, and they scatter the electrons or cause leakage current. Therefore it can significantly lower the electronic properties in MOSFET applications.

In this study, we prepared a $Si_4O_5N_3$ layer through several successive treatments of Si-adsorption, NO exposure, and oxidation on a SiC(0001) surface in an ultra-high vacuum (UHV) chamber. The structure was confirmed through quantitative low-energy electron diffraction (LEED) analysis, Auger electron spectroscopy (AES), and scanning tunneling microscopy (STM) observation.

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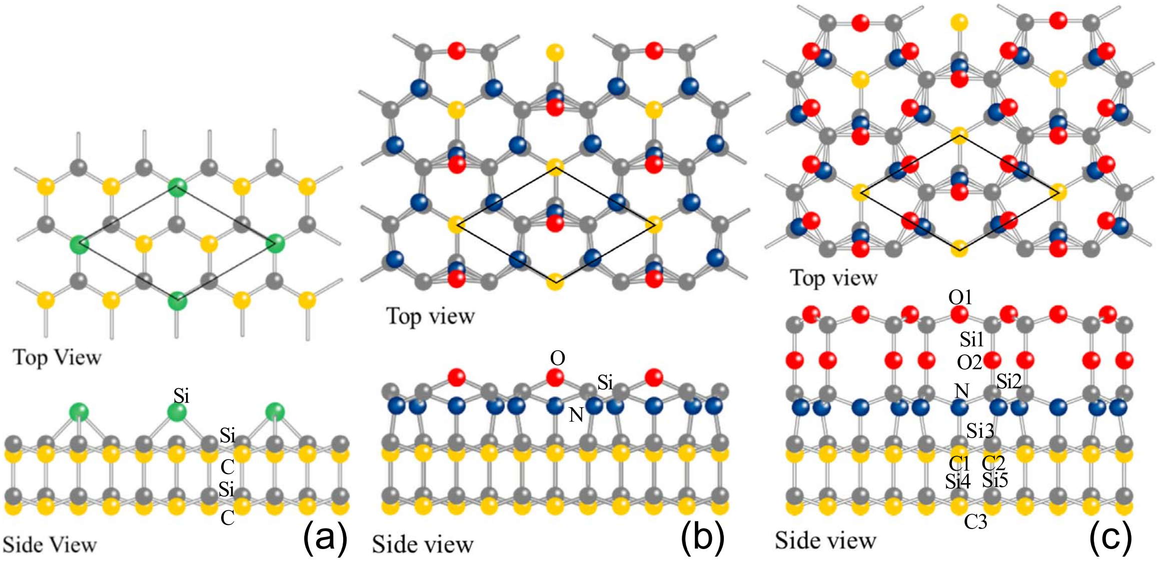

Fig. 1. Structural models of (a) SiC(0001)–$(\sqrt{3}\times\sqrt{3})R30°$–Si surface, (b) SiC(0001)–$(\sqrt{3}\times\sqrt{3})R30°$–$Si_2ON_3$ surface, and (c) SiC(0001)–$(\sqrt{3}\times\sqrt{3})R30°$–$Si_4O_5N_3$ surface.

2. Experiment

A single-crystal 6H-SiC(0001) wafer of width and length 3 mm × 10 mm and thickness 0.5 mm was pretreated by H_2-gas etching at 1360 °C for 30 min in the cold-wall reactor of a quartz furnace under atmospheric pressure to remove scratches on the wafer surface [18]. The sample was then clamped by tantalum plates on molybdenum blocks insulated by an aluminum nitride sheet for resistive heating in an UHV chamber. The sample holder was mounted at the end of the tube and cooled down by introducing liquid nitrogen into the tube. The chamber was equipped with LEED and AES optics (SPECTALEED, Omicron) in which the base pressure was better than 1×10^{-8} Pa with magnetic shields. The temperature of the sample was measured using a thermo-spot sensor (FTZ6, Japan Sensor). NO and O_2 gases were introduced into the chamber via variable leak valves. The sample was cleaned via cycling of silicon deposition and annealing at 1100 °C in UHV. The Si atoms were evaporated from a high-temperature Si wafer heated by direct resistive heating. The obtained surface was studied by LEED $I(E)$ analysis and AES measurement in the same chamber. For the STM observation, we used a separate UHV chamber equipped with a low-temperature STM (Unisoku). The sample was transferred from the LEED chamber to the STM chamber through the air. STM *I-V* measurements were performed at liquid nitrogen temperature.

The LEED spot intensities were measured using a digital charge-coupled device camera (ORCA-05G, Hamamatsu) with a computer-controlled data acquisition system [19]. A sample temperature during the measurement was 90 K. For structural analysis, the $I(E)$ curves of the LEED spots were measured within an incident energy range of 50–500 eV in 1 eV steps. A Barbieri–Van Hove symmetrized automated tensor LEED package was used to determine the atomic positions [20]. Thirteen phase shifts were used to represent atomic scattering. The damping of incident electrons was represented by the imaginary part of the inner potential, V_{0i}, of −5.0 eV, with Pendry's reliability factor (R_P) used to direct the automated search algorithm [20,21]. The best agreement between experimental and theoretical $I(E)$ curves was determined by minimizing R_P, with errors in the structural parameters estimated from the variance of R_P, $\Delta R = R_P(8|V_{0i}|/\Delta E)^{1/2}$ [21].

3. Results and discussion

3.1. Growth procedures

Our procedure to fabricate a $Si_4O_5N_3$ layer on a 6H-SiC(0001) surface in UHV was as follows. First, we prepared a Si-covered surface through Si deposition and annealing; the amount of Si was not essential, as we deposited a greater than sufficient amount and removed any excess through annealing at 1100 °C. By increasing the annealing time we could obtain an initial (3×3) LEED pattern that could be changed to a $(\sqrt{3}\times\sqrt{3})R30°$ LEED pattern using Si desorption. The annealing time depended on the amount of deposited Si but was typically 1 min for a (3×3) pattern and 5 min for a $(\sqrt{3}\times\sqrt{3})R30°$ pattern. The (3×3) and $(\sqrt{3}\times\sqrt{3})R30°$ structures are Si-rich and Si-poor, respectively [7,8,22]. The (3×3) surface, referred to here as the (3×3)-Si surface, had larger amount of Si adatoms than the $(\sqrt{3}\times\sqrt{3})R30°$ surface, which is referred as the $\sqrt{3}$-Si surface. A structural model and LEED pattern of the $\sqrt{3}$-Si surface is shown in Figs. 1(a) and 2(a), respectively. By applying this process to a surface covered by graphene layers, we were able to repeatedly obtain a Si-covered surface.

Next, we fabricated a Si_2ON_3 layer [11]. To do this, we used the Si-poor $\sqrt{3}$-Si surface. A well-ordered $\sqrt{3}$-Si surface was exposed to NO at 950 °C and a pressure of 5×10^{-5} Pa. This process typically required 30 min to produce a clear LEED pattern, which remained $(\sqrt{3}\times\sqrt{3})R30°$, as shown in Fig. 2(b), but was clearly distinguishable from the $\sqrt{3}$-Si surface through a comparison of respective intensity versus energy curves [$I(E)$ curves] or LEED patterns at suitable energy (e.g., at 120 eV), as shown in Fig. 2(a) and (b). If this process was started from a (3×3)-Si surface, the same structure would be obtained but the observed $(\sqrt{3}\times\sqrt{3})R30°$ LEED pattern would be weak and broad. The (3 × 3)-Si structure had 13 Si adatoms on the SiC(0001) crystal truncated (Si terminated) surface in the unit cell, which corresponds to 4.3 Si adatoms in the $(\sqrt{3}\times\sqrt{3})R30°$ unit cell, whereas the $\sqrt{3}$-Si surface had a single Si adatom in the unit cell. This result indicates that the number of Si adatoms in the (3×3)-Si surface is too large to form a well-ordered Si_2ON_3 layer. A structural model of the Si_2ON_3 surface is shown in Fig. 1(b).

Following this step, Si atoms were deposited onto the Si_2ON_3 surface. To improve reproducibility, we deposited the same amount of Si as in the first step of this study and annealed the sample at 1100 °C to adjust the number of Si atoms on the Si_2ON_3 layer to obtain the (3 × 3) LEED pattern shown in Fig. 2(c). The typical annealing time was 1 min. Although we have not analyzed its structure yet, the $I(E)$ curves of this (3 × 3) structure differ from those of the Si-rich structure, (3 × 3)-Si. If it were possible to deposit appropriate numbers of Si atoms onto the Si_2ON_3 layer, the annealing process might be unnecessary; however, although we have tried to adjust the Si deposition time and skip post-annealing, we have not yet obtained suitable results.