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Towards a framework for designing applications onto hybrid nano/CMOS fabrics

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ABSTRACT

The design of CAD tools for nanofabrics involves new challenges not encountered with conventional design flow used for CMOS technology. In this paper, we propose to define a new framework able to help the designer to map an application on a wide range of emerging nanofabrics. Our proposal is based on a variety of models that capture as well as isolate the differences between these fabrics. This tool supports the design flow starting from behavioral description up to final layout. It integrates fault-tolerant techniques and fabric-related density transformations with more conventional design automation techniques. After an overview of common requirements, physical models, and associated techniques, a case study in the context of NASIC fabrics is used to illustrate some of the concepts.

1. Introduction

As an alternative to CMOS based designs, novel nanofabrics are being proposed based on a combination of lithographic processes and bottom-up self-assembly based manufacturing. These fabrics include NanoPLA [1,2], CMOL [3], FPNI [4], and NASIC [5]—to name a few. They are based on a variety of devices such as FETs, spin-based devices, diodes, and molecular switches. Furthermore, all these architectures include some support in CMOS: some like FPNI would move the entire logic into CMOS, others, like NASIC, would only provide the control circuitry in CMOS. The rationale for this varies but includes targeted application areas as well as manufacturability issues.

Other differences include fault handling: e.g., some proposals would use reconfigurable approaches, while others like NASICs would rely on built-in techniques based on redundancy, voting, error correction, and/or unique fabric structures. The architectures proposed range from general purpose processors to programmable logic arrays similar to FPGAs, and to more specialized devices such as cellular arrays and cellular neural networks.

In order to implement an application on a nanofabric, specific tools are already proposed by the respective research groups [1,5,6] as CAD tools are necessary to be able to design and evaluate the capabilities of larger-scale systems. As the underlying technologies are still evolving according to advances in devices, manufacturing, and fabric structures, CAD tools for nanofabrics should be made, ideally generic enough to integrate added features or to enable new paradigms as well as comparison between various approaches.

This paper proposes a prototyping CAD tool that considers an explicit specification of the underlying nanofabric. It extends the classical design flow—shown in the Fig. 1—for designing an application from behavioral specifications (e.g., in VHDL, Verilog, or SystemC) onto physical designs. It is based on a range of transformations applied at different levels of description/abstraction of the application/problem that is mapped.

The new design flow proposed incorporates a variety of models associated with the nanofabric to allow optimizations to occur on generic data structures. Through a computational model, an architectural model, a technological model, and a fault model key aspects of a particular fabric can be captured and abstracted. The proposed models interact with the behavioral and the physical tools to produce an abstract layout for the design—starting from a high-level description. Parts that are mapped to nanoscale are separated from parts that use conventional CMOS technology.

Nanoscale fabrics under consideration have the following features:

- The use of self-assembly based manufacturing techniques, e.g., nanopatterning, fluidic alignment, DNA-based self-assembly,

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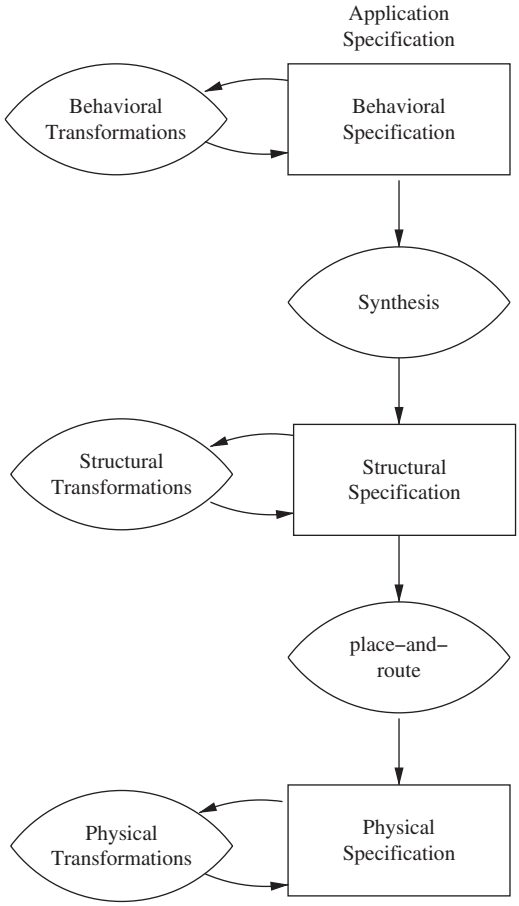

Fig. 1. Classical design flow of a conventional CAD tool.

and di-block co-polymers, in conjunction with conventional lithography: this is driving their structure to be quasi-regular such as based on 2-D crossbars.
- Nanoscale fabrics could be hybrid nano/CMOS structures as opposed to just nanoscale.
- Nanoscale fabrics are expected to have high defect rates, e.g., in the range of 10+%; thus, defect tolerance techniques need to be incorporated and taken into account in the design of any new CAD tool. In comparison, conventional CMOS designs in 90 nm technology have only 0.4 defects per cm^2.

The need to build a new framework able to support large applications based on emerging fabrics is apparent. While not all of the physical constraints are finalized, investigations have began and significant progress is made on all areas. We can expect that the development of a nano CAD framework can reduce the design gap between nanoscale designs and CMOS counterparts. As known, the classical tools are able to map millions of transistors large designs into CMOS technology.

In summary, this paper makes the following key contributions: (1) we propose to develop a new framework able to manage hybrid CMOS/nano architectures based on model specifications; and (2) the classic design-flow is extended to interact with these new models based on new and adapted tools/algorithms. Our broader objective is to develop a framework that could be used by research groups in this field and that could help them in their investigation of new materials, devices, and architectures evaluating implications at the system level.

The paper is organized as follows. Section 2 presents the proposed models used by this CAD framework to capture the characteristics of the nanofabrics. Section 3 gives an overview of the general organization of the proposed CAD framework. The subsequent sections discuss the main components of the new design flow. The last section shows the feasibility of the approach by taking an example application dedicated to NASIC nanofabric.

2. Models for fabric specification

The prototyping tool presented here is henceforth referred to as NanoMadeo. It is based on four meta-models. These meta-models provide abstractions of the nanofabrics concerning their computation paradigm (*computational meta-model*), their structural organization (*structural meta-model*), technological constraints (*technological meta-model*), and their fault-tolerance ability (*fault meta-model*).

Through these, the designer is able to capture different aspects of the target fabric. These models interact with behavioral transformations, structural transformations, and physical tools, needed to design and to implement an application onto the nanofabric support. These interactions are mediated by the meta-models. The aspects that need to be captured by the meta-models are detailed in the following subsections. The general flow of this tool is presented in Section 3.

2.1. Computational meta-model

CAD tools for emerging nanofabrics must be able to handle both traditional CMOS and nanoscale technologies. The distribution of functionality between the two depends on the nanoscale capabilities, manufacturability constraints, the trade-offs between area, performance, and the reliability of the underlying nanoscale technology.

For instance, the nanoscale parts of the system can be used solely for computation in order to gain orders of magnitude improvements in density and performance compared to CMOS technology [7]. Nanoscale technology could also be utilized for interconnect-only to speed-up communication in the fabric by reducing load capacitances and allowing a denser interconnect structure. A prototyping tool must handle both of these cases and in-between in order to be useful.

The computational meta-model also needs to be able to model different roles for the nano and/or CMOS segments related to both computation and interconnect. This partitioning is a new requirement of hybrid, i.e., nano/CMOS, fabrics that is not present in conventional tools.

2.2. Architectural meta-model

The architectural meta-model provides support for describing the building blocks of a target nanofabric. These building blocks correspond to nanoscale or CMOS components necessary to build the architecture on the fabric. These can be classified into basic devices, pre-composed blocks and wires as shown in Fig. 2. The architectural meta-model allows the specification of the types of tiles specific to each fabric: nanoBlocks for NanoPLA [1], tiles of basic cells for CMOL [3], hypercells for FPNI [4], and tiles for NASIC [5]. The topological organization of the nano and microcomponents, including their hierarchical structure in tiles, can also be captured by a model based on this meta-model.

2.3. Technological meta-model

The technological meta-model permits to model the physical constraints of the fabric based on the underlying technology. This