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High-aspect ratio through-silicon vias for the integration of microfluidic cooling with 3D microsystems

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ABSTRACT

Microfluidic cooling technology is a promising thermal solution for high-performance three-dimensional integrated circuits (3D ICs). However, the integration of microfluidic cooling into 3D ICs inevitably impacts tier-to-tier through-silicon vias (TSVs) by increasing their length and diameter (for a fixed aspect ratio). To address this challenge, this paper presents the fabrication of very high-aspect ratio (23:1) TSVs within a microfluidic pin-fin heat sink using two types of silicon etch masks. Void-free TSVs are electrically characterized using X-ray inspection and four-point resistance measurements.

1. Introduction

Three-dimensional integrated circuit (3D IC) technology has recently attracted considerable interest as a "More-than-Moore" solution [1,2]. The through silicon via (TSV) is a key component of 3D ICs; it offers decreased latency, decreased energy-per-bit, and increased bandwidth density [3–5]. However, one of the existing limitations to the realization of high-performance 3D ICs is the difficulty to dissipate generated heat since 3D ICs have limited thermal paths to the ambient compared to two-dimensional (2D) ICs. To this end, interlayer microfluidic cooling is widely explored as a means to address these thermal constraints. Microfluidic cooling was first shown by Tuckerman and Pease in 1981 [6], and since then, additional studies have presented the feasibility of microfluidic cooling for removing heat in single- and multiple-tiered chips [7–10].

When it comes to the integration of microfluidic cooling within 3D ICs, TSV aspect ratio is a key parameter that determines TSV electrical parasitics. Typically, to achieve higher cooling capability, a microfluidic heat sink requires each chip to be relatively thick, since the height of the heat sink is strongly related to its cooling capability. In prior work, the thickness of dice with an embedded microfluidic heat sink was shown to be a few hundred micrometers [6–11]. While such thickness is attractive from a thermal point of view, this inevitably increases TSV dimensions (diameter and height) and thus, TSV capacitance, which impacts latency and energy dissipation. Moreover, as a TSV diameter increases, the number of TSVs that can be placed in a heat sink, or a bandwidth density of I/Os, quadratically decreases between stacked ICs. Thus, small TSV dimensions are preferable since they not only minimize the silicon real-estate footprint, but they also improve the electrical performances. While prior work has shown the integration of TSVs in a microfluidic heat sink [9,11], the reported TSVs were very large in diameter (50–60 μm) and with an aspect ratio of only 5:1, leading to large electrical parasitics. Prior work [10] shows preliminary effort in the fabrication of 18:1 aspect ratio TSVs within a microfluidic heat sink. However, these TSVs were not electrically isolated and were not completely etched through the wafer due to innate difficulty in high-aspect ratio silicon etching and copper filling for a thick silicon substrate. Prior work [12] shows preliminary efforts on the integration of microfluidic cooling with 3D ICs. In addition, different approaches to the formation of high-aspect ratio (HAR) TSV fabrication have been proposed including nickel wires or wire bonds [13,14]. However, these TSV techniques require additional fabrication steps for BCB polymer formation between the TSV cores and the silicon.

This paper focuses on the fabrication of the fully isolated TSVs with an aspect ratio of 23:1 and investigates the integration of the HAR TSVs within a microfluidic heat sink using various fabrication processes. In Section 2, we propose a 3D system with TSVs embedded within interlayer-microfluidic cooling. Section 3 describes the fabrication in detail and electrical characterization of HAR TSVs within a micropin-fin heat sink; this is done using two different masking methods during the silicon etching step. Void-free TSVs are validated using four-point

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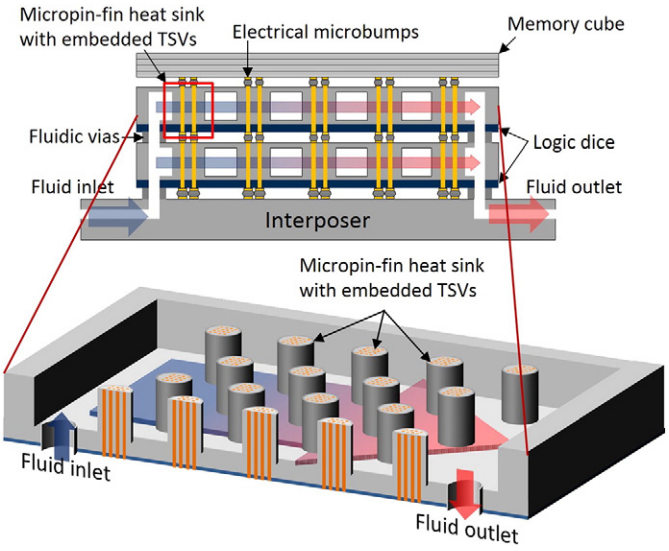

Fig. 1. A schematic of the proposed 3D system with embedded microfluidic cooling.

resistance measurements and X-ray imaging, and conclusions are presented in Section 4.

2. A proposed 3D microsystem: Need for high-aspect ratio TSVs

Fig. 1 illustrates a potential 3D electronic microsystem in which two logic dice and a memory cube are stacked on an interposer substrate. Each logic die consists of a micropin-fin heat sink with integrated TSVs for electrical connectivity. Fluidic vias are also formed in the dice

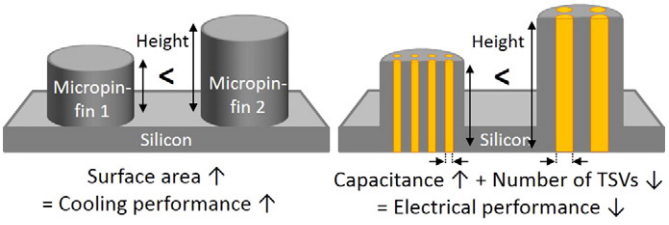

Fig. 2. Trade-off exists between electrical and thermal performances with respect to the height of silicon micropin-fins.

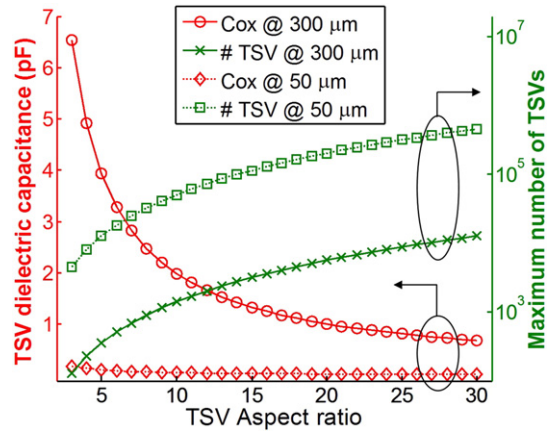

Fig. 3. TSV dielectric capacitance and maximum number of TSVs as a function of aspect ratio and die thickness (TSV diameter and oxide thickness are 13 and 0.5 μm, respectively).

Table 1
The dimension of TSVs and micropin-fins.

Dimensions	Diameter	Height	Pitch
Micropin-fin	150 μm	270 μm	225 μm
Through-silicon via	13 μm	300 μm	24 μm

to enable coolant delivery in and out of the dice. In such 3D ICs, the thickness of the silicon must be greater than the height of the micropin-fin heat sink. In general, micropin fins of a relatively large height are required in order to maintain an acceptable chip junction temperature under large power dissipation since the surface area of a heat sink increases as the heat sink height increases [10]. Moreover, it increases the hydraulic diameter of the heat sink and thus reduces the pressure drop. However, from an electrical perspective, this increased die thickness results in increased TSV dimensions (diameter and height) for a fixed aspect ratio TSV, as illustrated in Fig. 2. This in turn exacerbates the capacitance of the TSVs. The dielectric capacitance of TSVs can be expressed as [15]:

$$C_{ox} = \frac{2 \cdot \pi \cdot \varepsilon_{ox} \cdot h_{TSV}}{ln\left(\frac{r_{TSV} + t_{ox}}{r_{TSV}}\right)} \quad (1)$$

where ε_{ox} is the permittivity of silicon dioxide, t_{ox} is the thickness of silicon dioxide, r_{TSV} is the radius of a TSV, and h_{TSV} is the height of a TSV, respectively. Fig. 3 illustrates TSV capacitance and the maximum number of TSVs as a function of TSV aspect ratio for two die thicknesses (50 and 300 μm), assuming only 1% of the die area is allocated for TSVs. For the thinner (50 μm) die, which is in line with conventional 3D ICs, increasing the TSV aspect ratio does not significantly improve TSV capacitance. However, for thicker (300 μm) die, which is in line with the thickness needed for dice with embedded microfluidic cooling, the TSV aspect ratio plays a critical role in the electrical performance. If we increase the TSV aspect ratio from 5:1 to 20:1, the TSV capacitance decreases from 3.94 pF to 1 pF (an approximately 75% reduction). At the same time, assuming only 1% of the die area is allocated to TSVs, the maximum number of TSVs in the die increases from 353 to 5658. Thus, for silicon die with embedded microfluidic cooing, it is important to develop HAR TSVs to lower the capacitance and increase the number of interconnections between the tiers. This is missing in the literature and the focus of this paper. The following section describes our proposed TSV processes and their integration with the silicon micropin-fin heat sink.

3. The fabrication of high-aspect ratio TSVs in micropin-fin heat sink

The fabrication of TSVs within micropin-fins begins with a 300 μm thick double-side polished silicon wafer to enable the fabrication of 270 μm tall micropin-fins with a diameter of 150 μm. As will be discussed in this section, we demonstrate a 1 cm^2 die with 1936 micropin-fins, each containing 16 TSVs in a four by four array. The fabricated TSVs are 13 μm in diameter and 300 μm in height, which yields an aspect ratio of 23:1. Table 1 summarizes the dimensions of TSVs and micropin-fins. Fig. 4 illustrates the overall fabrication steps for HAR TSVs in micropin-fins. Fig. 4(a) illustrates a HAR silicon via etching step using two etch masks (either by an oxide mask or a photoresist mask), and Fig. 4(b) presents the fabrication processes following silicon via etching.

3.1. High-aspect ratio silicon via etch using two etch masks

The first step of the process is to etch narrow and tall silicon vias using the Bosch process, which alternates between passivation (C_4F_8) and etching (SF_6). This process step requires a precise procedure because the total area of vias to be etched is extremely small (e.g., 0.32%), which leads to a