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New design of RF rectifier for passive UHF RFID transponders ☆

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ABSTRACT

A novel diode-connected MOS transistor for ultra-high-frequency (UHF) micro-power rectifiers was presented, and a high efficiency *N*-stage charge pump voltage rectifier based on this new diode-connected MOS transistor was designed and implemented. The new diode-connected MOS transistor and the rectifier are designed and fabricated in SMIC 0.18-μm 2P3M CMOS embedded EEPROM process. The structure design of the new diode achieved 315 mV turn-on voltage, and 415 nA reverse saturation leakage current. Compared with traditional rectifier, the rectifier using the presented diode-connected MOS has higher power conversion efficiency (PCE), higher output voltage and smaller ripple coefficient. When the RF input is a 900-MHz sinusoid signal with the amplitude ranging from 0.8 to 1.8 V, PCEs of the charge pump rectifier with only 3-stage are more than 30%, and the maximum output voltage is 5.02 V, and its ripple coefficients are less than 1%.

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1. Introduction

The rapidly increasing range of application of radio frequency identification (RFID) technology includes supply chain management, access control to buildings, public transportation, airport baggage, and express parcel logistics [1–3]. Using an RFID system is a good approach for automated identification of products. The need for lower cost, higher data rates, and longer reading distances is increasing, while stringent regulation of transmit power and bandwidth have to be met.

RFID tags (or transponders) are often classified as passive or active. The passive tag is energized by an electromagnetic radio frequency (RF) wave transmitted by the reader, while the active tag is energized by a battery. Passive tags have the virtues of low cost and long life. As the passive tag is remotely powered by a reader's RF signal, it must be able to operate at very low power levels (∼μW) [1]. The ultra-high-frequency (UHF) passive RFID tag has to work at a considerably long distance from the transmitter (or reader). As the RF energy received by the tag decreases rapidly with distance, the induced voltage across the tag antenna is often very small [4–6]. In order to obtain a high output voltage, an *N*-stage voltage rectifier (or called charge pump multiplier) is typically used [1,7,8]. Schottky diodes with low potential barrier are widely used for achieving a high output voltage and a high power conversion efficiency (PCE), but standard CMOS process has not Schottky diodes. Instead of Schottky diodes, the diode-connected MOS transistors with very low threshold voltage are used in the *N*-stage voltage multiplier [4–5]. The shortcoming of using MOS transistors is that the threshold voltage is increased by the body effect. As of today, even though many design techniques for the RF rectifier using diode-connected MOS transistors shown in Fig. 1 have been reported [4–5,9–12], the minimum input voltage level and the PCE of the rectifier using diode-connected MOS transistors are less beneficial than those of the rectifier using Schottky diodes. For example, the design strategy and efficiency optimization of ultrahigh-frequency (UHF) micro-power rectifiers using diode-connected MOS transistors with very low threshold voltage is presented in [4], but [4] has not solved the problems generated by the substrate bias effect of diode-connected MOS transistors.

In this paper, a novel diode-connected MOS transistor for the rectifier was presented, and a high efficiency *N*-stage charge pump voltage rectifier circuit based on this new diode-connected MOS transistor was designed and implemented. Section 2 starts with the design of a new diode-connected MOS transistor. Section 3 discusses the parasitic effect and design optimization of the new diode-connected CMOS.Section 4 gives simulation results for the *N*-stage rectifier using the novel diode-connected MOS transistor. Section 5 concludes our research efforts.

2. Design of a new diode-connected MOS transistor

When replacing diode with diode-connected MOS transistor, we have to assure that the new structure will turn on when it is forward-biased and will cut off when it is reverse-biased. So not only the substrate of NMOS should connect to the lowest voltage, but also the substrate of PMOS should connect to the highest voltage.

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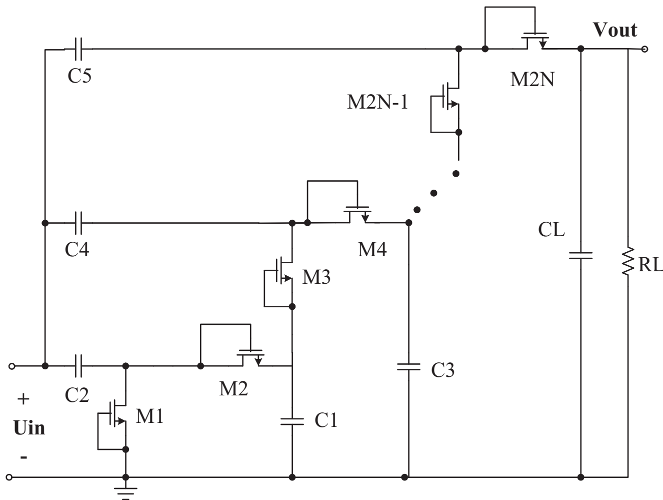

Fig. 1. Traditional CMOS charge pump rectifier.

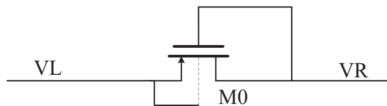

Fig. 2. Diode-connected PMOS.

As shown in Fig. 2, the substrate of a diode-connected PMOS is connected to its source. Then, when VL is higher than VR, there will be a current from VL to VR, which means that the diode turns on when it is forward-biased. On the other hand, when VR is higher than VL, the voltage of drain is higher than that of the substrate, the drain–body junction starts to conduct, which means that the diode does not cut off when it is reverse-biased.

This can be solved by connecting the substrate of PMOS to the *highest voltage*. But there will be two problems in practice:

1) MOS transistor works in dynamic status, so it is difficult to decide the *highest voltage*.
2) Substrate bias effect will result in the increase of the threshold voltage, and make the turn-on voltage increase ultimately.

The structure of improved *diode-connected CMOS* for substituting the Schottky diode is shown in Fig. 3. The *improved diode-connected CMOS* could decrease the turn-on voltage and ensure that the substrate is connected to the *highest voltage*.

In Fig. 3, M0 supplies an exiguity bias current via bias voltage BIAS. So VG will bias at a level of $VR-V_{TH}$, where V_{TH} is the drain–body junction turn-on voltage.

PMOS M2 and M3 are used to assure that the substrate of M1 is connected to the highest voltage. If VL is higher than VR, M2 will turn on while M3 will cut off, and the potential of M1, M2 and M3's substrate VSUB will rise up to VL. Otherwise, if VR is higher than VL, M3 will start to conduct while M2 will cut off, and the potential of M1, M2 and M3's substrate VSUB will rise up to VR. All these ensure that the substrate of M1, M2 and M3 is always connected to the highest potential, so that the drain–body junction is reverse-biased all the time.

Now, let us have a look at the working principle of the whole structure. When VL is high, M1 works in linear region and the turn-on resistance is small, so VR can be as high as VL. On the other hand, when VL is low, VG is about $VR–V_{in}$, The absolute value of V_{GD} of M1 will be smaller than its threshold voltage, and M1 will cut off. In this way, we realize a diode which will turns on when it is forward-biased with small voltage. Using SMIC

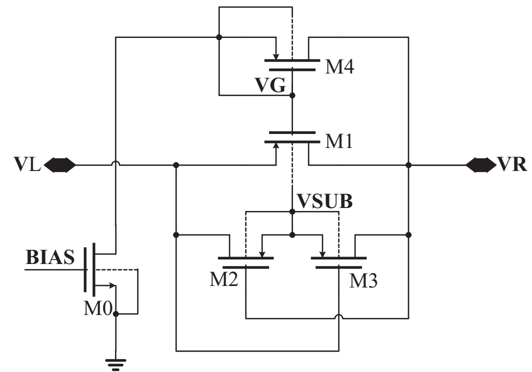

Fig. 3. The schematic diagram of improved diode-connected CMOS.

0.18-μm 2P3M CMOS embedded EEPROM process, in this diode, M0 is high-voltage zero-threshold NMOS, whose threshold voltage is 0.31 V. M1, M2 and M3 are all high-voltage PMOS, whose threshold voltage is −0.92 V. The drain–body junction turn-on voltage of all these transistors is 0.7 V. It is notable that the absolute value of the threshold voltage V_{TH} of the PMOS is higher than the drain–body junction turn-on voltage V_{th}.

3. Analysis and optimization of the new diode-connected CMOS

M2 and M3 always work in linear region, in order to connect the substrate voltage. So they don't need big (W/L), actually, it is *2/1* in this design. For M1, if the number of the multiple transistors is bigger, i.e., the W/L will be bigger, the turn-on resistance will be smaller, and then the turn-on voltage will be lower. However, bigger (W/L) bring in greater reverse leakage current. So we need a tradeoff among forward turn-on voltage, reverse leakage current and area. Fig. 4 shows the different turn-on voltage (when conduction current is 100 μA) and different reverse leakage current (when reverse voltage is 1 V) with different number of parallel connection transistors. In Fig. 4, we can see that the reverse leakage current get greater with the increase of the number m of parallel connection transistors, and the reverse current is directly proportional to the m. From the analysis above, 10 could be the probable number of multiple transistors. When the number is 10, the turn-on voltage is only 315 mV, and the reverse leakage current is 415 nA. This new diode-connected CMOS has some advantages:

1) The problem of body-potential connecting is solved by body-switching technique.
2) The control of M1's gate voltage is realized by a simple bias circuit, which makes M1 be in linear region rather than saturation region when it is turned on. Therefore, this structure has a small forward voltage, which is applicable to UHF RFID tag. It is also showed in Fig. 4 that the forward voltage is only 0.3 V when the size of M1 is carefully adjusted. When the voltage amplitude of the antenna in UHF RFID tag is small, high conversion efficiency and high output voltage is important to rectifier of UHF RFID tag.

Now, let us have a look at the influence of the gate-source parasitic capacitance on circuit performance.

As shown in Fig. 3, C_P=Cgs1 is a relatively large parasitic capacitance, and is about 0.1 pf. When VL changes, because of the coupling of C_P, the gate voltage of M4–VG will change too. Two assumptions are analyzed here under the condition that the RF input was a 900-MHz sinusoid.

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