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Design and simulation of sequential circuits in quantum-dot cellular automata: Falling edge-triggered flip-flop and counter study

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is an emerging nanotechnology, with extremely small feature size and ultralow power consumption comparing with transistor-based technology. Anteriority, basic level-triggered flip-flop designs based on QCA implementation were examined. In this paper, we utilize the unique QCA characteristics and clock zones to design falling edge-triggered *J-K* flip-flop that is stable and practical. Simulation with the QCADesigner simulator is performed to verify the functionality of the proposed falling edge-triggered flip-flop. This paper also explores the design of counters. Synchronous counters are designed with several different bit sizes and simulation results demonstrate the validity of them.

1. Introduction

As conventional CMOS technology hits its fundamental feature size limit, recent years have seen a number of research efforts that have focused on new devices that might replace CMOS technology [1]. One of the promising emerging devices is Quantum-dot Cellular Automata (QCA) [2–5]. Originally proposed by Lent et al. [2], QCA uses arrays of coupled quantum dots to build Boolean logic functions [6] and to perform useful computations. So QCA not only offers a solution to bottleneck of scaling feature size, but also a new way of information transformation. Moreover, conventional digital technologies use ranges of voltage or current to represent binary values. In contrast, QCA uses the position of electrons in quantum dots to represent binary values 0 and 1. Consequently, the primary advantages of QCA are the exceptionally high logic integration derived from the small size of dots, and with the notably low power consumption.

QCA can be used to implement combinational circuits by properly arranging cells in series. So far, several studies have been reported about combinational circuit design, such as QCA Full Adder [7,8], Multiplexer [9] and Programmable Logic Array [10], etc. At the same time, memory circuits have also attracted some attentions, such as QCA random access memory [11] and serial memory [12], etc. Actually, flip-flops are also very important quantum-dot cellular automata (QCA) circuits because they are expected to be used for designing and realizing large scale sequential circuits, for example counter. Anteriority, some works about sequential circuits design have been published, like QCA *R-S* flip-flop [9,13,14], *D* flip-flop [13–15] and Semaphore sequential circuit [13]. But to our knowledge, QCA flip-flop and sequential circuit designs have not been widely studied. The objective of this paper is to propose two detailed falling edge-triggered design by utilizing special QCA clock zones with an input Clock Pulse (*CP*) to realize *J-K* flip-flop (*J-K* FF). Ulteriorly, counter designs have not been considered by QCA designers. As an application to falling edge-triggered *J-K* flip-flop, QCA *n*-bit synchronous counters and their characters are examined. QCA sequential design schemes are inherently pipelined and require device and clocking methodology that differs significantly from conventional CMOS designs. Due to the importance of the QCA clock in creating actual designs, it will be discussed in detail in Section 2.

This paper is organized as follows: In Section 2, a brief background of QCA technology and its clock phase scheme and clock zone signal are presented. In Section 3, the design and implementation of falling edge-triggered and *J-K* flip-flop are shown. In Section 4, as an application of the proposed *J-K* flip-flop to sequential circuits, *n*-bit QCA synchronous counters are presented. In Section 5, simulation results and different bit size counters characters are shown. Conclusions are given in the last Section.

2. QCA review

The basic building block of QCA devices named *cell* is presented in Fig. 1(a). QCA cell consists of four quantum dots in a square array coupled by tunnel barriers, two electrons are injected into the cell. Due to Coulombic repulsion, the

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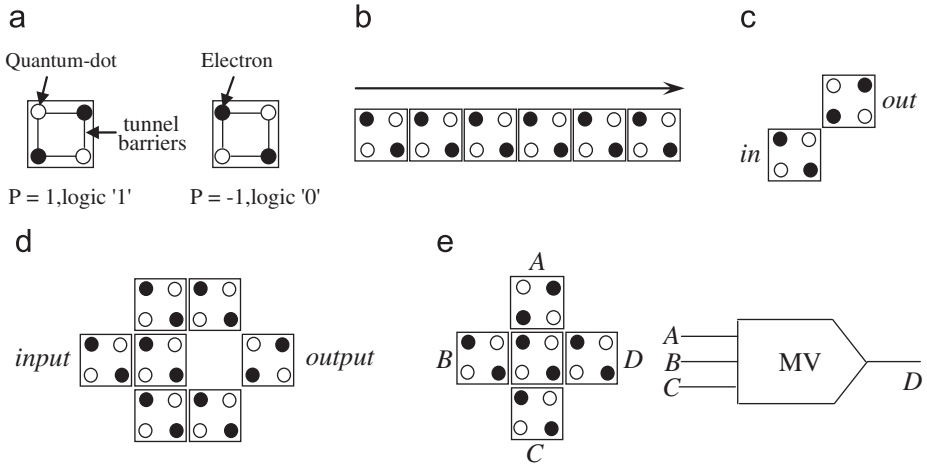

Fig. 1. Basic QCA logic devices. (a) cell; (b) wire; (c) and (d) inverter; (e) majority voter (MV).

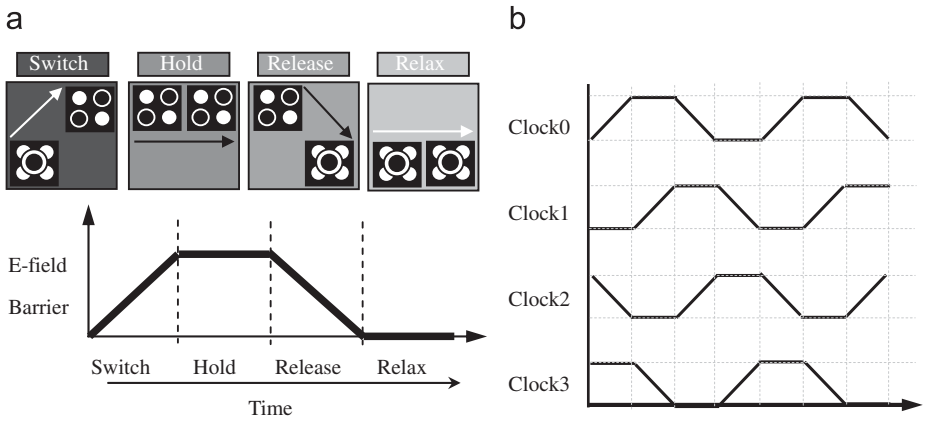

Fig. 2. (a) Four phases of the QCA clock [17]. (b) Clock zones signal.

two electrons reside in opposite corners representing two polarizations [16].

2.1. QCA logic

Some basic elements for QCA logic implementation are wire, inverter, and majority voter [4] shown in Fig. 1. QCA wire is formed by an array of QCA cells shown in Fig. 1(b), which provides a medium for data propagation based on Coulomb interactions. The simplest inverter is built by placing QCA cells in a diagonal structure shown in Fig. 1(c); the common inverter is built by seven cells shown in Fig. 1(d). The polarization of the output QCA cell '*out*' or '*output*' is the opposite of the polarization of input QCA cell '*in*' or '*input*'. QCA majority voter (MV) and its logic symbol are shown in Fig. 1(e), MV, is equivalent to a logic function $F(A, B, C)=AB+AC+BC$ and can be implemented by five QCA cells arranged in a cross. Cells *A*, *B*, and *C* are input cells, and cell *D* is the output cell that is polarized according to the polarization of majority of the input cells. For example, since two (out of three) input QCA cells are polarized to -1, the output cell is also polarized to -1 (see Fig. 1(e)). Logical AND and OR functions can be implemented from majority voter by presetting one input immutably to binary values 0 and 1, respectively.

2.2. QCA clocking

A QCA cell has four clock phases; they are Switch, Hold, Release and Relax [17]. Fig. 2(a) shows its operation process. During the switch phase, QCA cells begin unpolarized and their interdot potential barriers are low. The barriers are then raised during this phase and the QCA cells become polarized according to the state of their driver (i.e. their input cell). It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunneling and cell states are fixed. During the hold phase, barriers are held high so the outputs of the subarray can be used as inputs to the next stage. In the release phase, barriers are lowered and cells are allowed to relax to an unpolarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an unpolarized state [16,17]. In the mean time, the large scale QCA circuit is partitioned into four clock zones; Fig. 2 (b) shows each clock zone signal and demonstrates pipeline mechanism. All cells in a certain zone are controlled by the same QCA clock signal. Cells in each zone perform a specific calculation; the state of a zone is then fixed so that it can serve as input signals to the next zone. Information transfers in a pipelined fashion.

3. QCA Edge-triggered *J-K* flip-flop design

In this section, falling edge-triggered mechanisms and its QCA implementation are discussed. Then *J-K* flip-flop is designed with falling edge-triggered structure. In all the design of this paper, QCA cells have a width and height of 18 and 5-nm-diameter quantum dots. They are placed on a grid with a cell