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Review Article

High resolution optical lithography or high throughput electron beam lithography: The technical struggle from the micro to the nano-fabrication evolution

Shinji Okazaki

Gigaphoton Inc., 400 Yokokurashinden, Oyama, Tochigi 323-8558, Japan

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ABSTRACT

The development of integrated circuits has been stimulated by the miniaturization of the device feature size on a chip. The development of lithographic technologies such as optical lithography and electron beam lithography made important contributions to this miniaturization. Resolution improvement is the most critical issue in the development of optical lithography. On the other hand, in the development of the electron beam lithography, the resolution excellent, but improvement in the throughput capability is the most critical issue. This paper describes the history of resolution improvement efforts in optical lithography and throughput improvement efforts in electron beam lithography through the development history of dynamic random access memories (DRAMs).

1. Introduction

Advances in ultra large scale integration (ULSI) technology have been facilitated by the miniaturization of the feature size of devices on an Si chip [1,2]. This miniaturization has been promoted by Moore's law and guided by Denaard's scaling theory [3,4]. Because of this miniaturization, the integration level of ULSI has become very high over the past 40 years. Micro-electronic Engineering has published many papers this miniaturization.

Fig. 1 shows the miniaturization trend of ULSI devices and the integration level of DRAMs (dynamic random access memories). Not only the integration level of ULSI devices, but also the performance of devices has improved drastically [5].

In the first 30 years, the miniaturization of ULSI was led by the development of DRAM devices [6]. This paper discusses the development of lithographic technology mainly through the perspective of the miniaturization of DRAM devices.

At the beginning of the 1970's, the minimum feature size of ULSI devices was approximately 10 μm or larger. The integration level in the DRAM devices was approximately 1 kb DRAMs. Currently the minimum feature size of the leading edge DRAM is below 30 nm and the integration level of the DRAM is over 4 Gb. This means that the integration level has become 10 million times larger than that of the DRAMs in the 1970's.

Various kinds of lithographic technologies were developed over the past 40 years [7–9]. Fig. 2 shows the evolution of lithography during this period. First, optical lithography was used in the contact printing scheme. In this scheme, the resolution limit was thought to be approximately 2–3 μm. There were also problems related to defects. In the contact printing scheme, the photomask and the resist coated wafer must be contacted. In such conditions, the particles in the environment could enter the resist layer and become defects [10,11]. To overcome this resolution limit and prevent defects, a projection exposure scheme with a scanning exposure scheme was introduced. At this point, there were no strict view of obtaining sub-micron patterns with optical lithography.

First, the one to one projection scheme with a full wafer scan system was introduced in the middle of the 1970's. In this system, a whole wafer had to be covered, and the numerical aperture (NA) could not be made large enough to obtain a higher resolution. Then we developed the reduction projection exposure scheme at the end of the 1970's. With the development of the reduction projection exposure system, the actual resolution improvement had begun [12].

Under such circumstance, we also tried to develop several new lithographic technologies as alternatives to optical lithography. Electron beam lithography is one of the candidates for post optical

E-mail address: shinji_okazaki@gigaphoton.com

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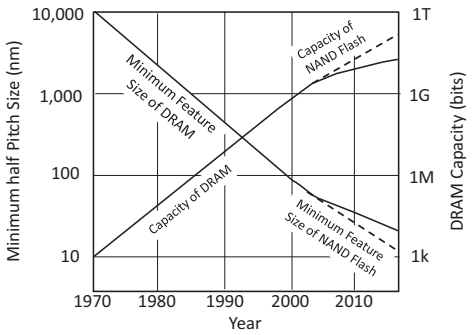

Fig. 1. Miniaturization trends of the DRAM/Flash devices and the Bit Capacity Trends of a DRAM/Flash Chips from 1970 to 2014. First 30 years, DRAM devices led the miniaturization. In recent years, NAND Flash memory devices succeeded the miniaturization trend of DRAM devices.

lithography. However, it was used for very limited applications such as the fabrication of very fine device for research purposes and for the fabrication of ASICs (application specific integrated circuits) and special logic devices used for the mainframe computers in the QTAT (quick turn-around time) lines [13–15]. It should be noted that the use of electron beam lithography for the fabrication of photo-masks began to be widely employed during this period [16].

X-ray proximity printing and ion beam lithography were also proposed as candidates of post optical lithography [17,18]. However, the development activities of X-ray lithography could not be continued because of resolution limit. The development of ion beam lithography also did not succeed owing to the limited throughput capability. Therefore, optical lithography and electron beam lithography continued to be developed. These efforts made important contribution to the developments of ULSIs. In this paper, the details of the developments of optical lithography and electron beam lithography will be discussed.

2. The development of optical lithography

As mentioned above, we have been using optical lithography for the fabrication of ULSIs in the industrial environment for more than four decades [19]. During this period, many declarations of the demise of optical lithography were made, but each time the technology was salvaged by the introduction of various resolution improvement techniques such as changes in the exposure scheme, improvements in optical systems, exposure wavelength reduction and resolution enhancement technologies. The details of these resolution improvements are described below.

2.1. The prelude to reduction projection optical lithography

Fig. 3 shows the resolution improvement history of optical lithography. In the first stage, we used the contact printing scheme for the fabrication of large scale integration (LSI) chips. In this scheme, a one to one contact mask was used. The masks were fabricated by employing the photo-repeater from the 10X reticle [20]. The reticles were fabricated by the pattern generators. By employing this one to one mask, a contact printer, and negative tone resist materials, we fabricated DRAMs for several generations such as 1 kb, 4 kb, 16 kb and 64 kb. We could delineate patterns down to several micron ranges by using this contact printing system. In this system, defect generation was the major issue. Because of the contact between the wafer and the mask, we could not eliminate the

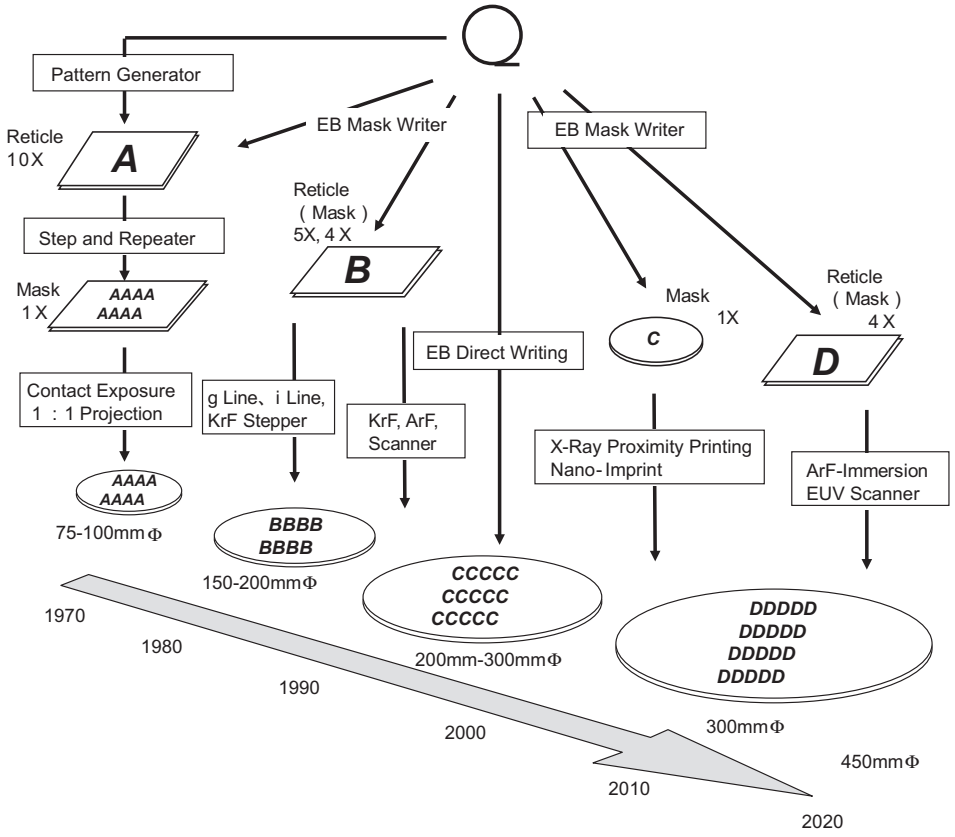

Fig. 2. Evolution of lithography. Various kinds of exposure schemes such as optical, EB, X-ray, and imprint were proposed. In the industrial environment, optical exposure schemes have been used for ULSI fabrication and EB has been mainly used for mask fabrication.