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Multilayer thin film capacitors by selective etching of Pt and Ru electrodes

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ABSTRACT

Capacitors and other passive components within electronic devices can significantly affect the size of electronic devices. To continue decreasing the size of electronics, the miniaturization and potential integration of capacitors require thin film technologies. However, the number of fabrication steps needed for many thin film multilayer capacitor fabrication methods is proportional to the number of active capacitor layers, rendering them cost and time consuming. To overcome this issue, we developed a method using the highly selective etching capability of platinum and ruthenium for the fabrication of multilayer thin film capacitors, resulting in a process which is independent of the number of capacitive layers. To demonstrate the process, one-, two-, and three-layer 2.5 mm × 2.5 mm devices were fabricated using a proof-of-concept silicon oxycarbonitride dielectric grown by plasma-enhanced chemical vapor deposition. The resulting 278 ± 3 pF, 508 ± 5 pF, and 762 ± 5 pF capacitors showed negligible frequency dispersion up to 1 MHz, and had low dissipation factors of ~0.001 at 10 kHz. As a demonstration of the versatility of the process, devices with thicker dielectric layers (3.5 μm) were also fabricated with a capacitance of 101 ± 2 pF which could achieve up to 640 V before the devices were permanently damaged. The versatility of the process suggests it is a good candidate for the future integration of multilayer capacitors, since it can potentially be fabricated by a variety of deposition methods, and can be formed on two- or three-dimensional substrates.

1. Introduction

Passive electronic components (resistors, inductors, and capacitors) are presently mounted on the surface of circuit boards and are connected through vias and highways of conducting paths embedded within the circuit board itself. These passive components can consume more than 40% of the circuit board area [1]. To obtain further reduction in electronic device size, research is being conducted to embed these surface-mounted passive components within the circuit board or integrated circuit (IC) packaging.

Current surface-mount capacitors are fabricated through ceramic processes. In short, a ceramic slurry is made into sheets, which are screen printed with electrodes and stacked numerous times. The stacked material is then pressed and diced into individual capacitors, followed by firing and a process to connect the electrodes [2,3]. Although significant improvements have been made to the fabrication process and material synthesis to achieve capacitors that are now 1 million times smaller than the same capacitance values achieved in 1961, the current processing technique is believed to be reaching its limitations. Therefore, extensive research is being performed on development of new dielectric materials as well as fabrication techniques. However, although materials with increased dielectric constant have been achieved with some success, many high-k materials have undesirable properties such as high leakage current, low breakdown strength [4], and/or voltage- or frequency-dependent capacitances [5], limiting the commercial viability. Therefore, it is of utmost importance to develop new fabrication processes to achieve further miniaturization of these devices.

Thin film deposition techniques promise to be the future of the miniaturization of passive component development, due to the ability to deposit uniform, dense, and smooth dielectric and metal layers, which are all factors which can significantly affect the performance and reliability of the current multilayer capacitor technology [2]. However, many of the recently reported multilayer capacitor thin film fabrication methods are disadvantageous in that the electrode layers are connected through a series of vias [6,7]. Therefore, the fabrication process is very cumbersome and adds a significant number of processing steps, increasing the

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probability of device failure and the overall cost of the device, as well as wasting valuable footprint area. In an attempt to overcome this issue, Imamiya et al. [8] demonstrated multilayer capacitors fabricated by magnetron sputtering through successive shadow masks to outline the features of alternating platinum electrodes and the barium titanate dielectric. However, shadow masks require smooth surfaces, can pose as a substrate or device scratching hazard, and the masking capabilities are not sufficient for CVD or atomic layer deposition processes.

To achieve a multilayer capacitor process which is more scalable, efficient, universal, and can be deposited from a variety of deposition systems, a process which does not require a separate patterning step for each layer is needed. Such fabrication processes have previously been visualized and patented in which two different electrode materials with highly selective etchants are alternated throughout the multilayer capacitor [9,10]. The concept is to make the full multilayer stack first, and only two or three patterning steps are needed to connect alternate electrode layers and create a capacitor with an arbitrary number of layers. However, these ideas have not been realized in the market today. The key to the success of this method is finding two electrode materials with isotropic etching processes which are extremely selective to only that material, and do not attack the other electrode material or the dielectric. Additionally, the electrode material would ideally have a high conductivity to reduce loss due to equivalent series resistances.

To this end, we have developed a process utilizing highly selective etching of two metals, platinum (Pt) and ruthenium (Ru), to significantly decrease the processing steps required in fabricating thin film multilayer capacitors. The current process was developed as a proof-of-concept approach in which the investigated dielectric layer (silicon oxycarbonitride) was deposited by plasma-enhanced chemical vapor deposition (PECVD), and the metal layers were deposited using sputtering. The advantage of this process is that all of the layers are deposited first, followed by the same top-down fabrication process regardless of the number of layers. This process could therefore be easily transferable to single systems or cluster tools to deposit all of the layers sequentially *in situ*, which would reduce the chance for defects or atmospheric contamination.

2. Materials and methods

2.1. Deposition of layers

Silicon (Si) wafers were used as the substrate for these devices. The Si substrates were cleaved into large pieces, typically ~2 in. × 6 in., and then rinsed in acetone, methanol, and isopropyl alcohol, sonicated in an acetone bath for 10 min, and placed in a dilute HF bath followed by rinsing in DI water and subsequent drying under blowing nitrogen.

A PECVD grown silicon oxycarbonitride (SiOCN) was chosen as the dielectric for the fabrication of the devices, the deposition parameters of which are described elsewhere [11]. In short, silane (15 sccm), methane (150 sccm), nitrous oxide (300 sccm), and hydrogen (1800 sccm) were introduced into an Applied Materials Precision 5000 PECVD deposition chamber at a pressure of 7 Torr, RF power of 400 W, and substrate temperature of 400 °C. SiOCN was chosen because of its good electrical properties (low leakage current and high breakdown strength), low residual stress, ability to deposit very thick films, and observed excellent chemical resistance to all of the etchants used throughout the process [11]. This material was chosen for fabrication proof-of-concept, and it should be mentioned that other materials will also be suitable for this process. In fact, SiO_2 and HfO_2 also show excellent etch resistance to the Ru and Pt etchants.

The Ru and Pt electrodes were deposited using a magnetron sputter deposition system (AJA International, Inc.). Both metals were sputter deposited to ~30 nm using a 2 in. target (Kurt J. Lesker) at 200 W RF power, chamber pressure of 4 mTorr, argon flow rate of 20 sccm, and target-to-substrate distance of 6 in. Titanium (~5 nm) was deposited before and after the Pt electrode for adhesion, but for simplification of the process description we will refer to this Ti/Pt/Ti layer as solely a Pt layer. Chromium (Cr) was sputtered for use as a dry etching mask and the sidewall electrodes, and was also sputtered using the same conditions as above except with a 3 in. target and 200 W DC power.

2.2. Electrical characterization

The capacitance and dissipation of the devices were measured using an Agilent 4284A LCR Meter. The measurements were performed at room temperature with an oscillating voltage of 30 V_{rms} and bias of 0 V. Two hundred data points were collected between a frequency range of 200 Hz to 1 MHz. The electrical breakdown strengths of devices with 1 μm thick dielectric layers were tested using current–voltage (I–V) measurements via a Keithley 6487 Picoammeter/Voltage Source with a 2.4 MΩ series resistance to protect the equipment at the time of failure. The voltage on the power supply was increased from 0 with steps of 1 V until breakdown was reached, averaging 10 current measurements per step, and holding the voltage for approximately 1 s before each step due to the time delay from system communications. Due to the higher voltage capabilities of devices made with 3.5 μm thick dielectric layers, these thicker devices were tested using the Keithley 6487 Picoammeter and a Keithley 248 High Voltage Power Supply. The high voltage setup also had the same 2.4 MΩ series resistance, but the voltage step was 10 V and system communication delay between each step was roughly 2 s.

3. Fabrication procedure

The fabrication procedure is achieved using a top-down approach after the deposition of all of the desired layers. Although the development of the process was achieved using two separate deposition systems, the process can be easily transferred to a system with the ability to deposit all layers *in situ*, which would increase the reliability of the process and decrease the probability of defects. Fig. 1 illustrates a simplified fabrication process flow, with a detailed description provided below.

The following steps were followed to deposit all of the layers to achieve the structure illustrated in Fig. 1(a) prior to device fabrication: (i) SiOCN was first deposited as an insulating layer on the Si substrate, (ii) a Pt layer was deposited as the first electrode, (iii) SiOCN was deposited again to a thickness of either 1 μm or 3.5 μm to test the changes in electrical properties from different dielectric thicknesses, (iv) a Ru layer was deposited as the second electrode, (v) SiOCN was deposited again to the same thickness as Step (iii), and (vi) the process was repeated from Step ii until the desired number of layers had been reached. The device finishes with a SiOCN deposition because this is also necessary for electrical insulation when the sidewall electrodes are deposited to connect alternate electrodes. We will refer to the devices tested within this work as one-, two-, or three-layer devices, which correspond to the number of active capacitive layers (*e.g.* a two-layer device consists of a Si substrate/SiOCN/Pt/SiOCN/Ru/SiOCN/Pt/SiOCN stack).

After deposition of all the layers was completed, a ~800 nm thick Cr mask was then sputtered and patterned on the stack into 2.5 mm × 2.5 mm squares using standard photolithography techniques. Cr was chosen as the mask material as it exhibited superior etching protection compared to photoresist or aluminum. All