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Simulated analysis for InGaP/GaAs heterostructure-emitter bipolar transistor with InGaAs/GaAs superlattice-base structure

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Abstract

A novel InGaP/GaAs heterostructure-emitter bipolar transistor (HEBT) with InGaAs/GaAs superlattice-base structure is proposed and demonstrated by two-dimensional analysis. As compared with the traditional HEBT, the studied superlattice-base device exhibits a higher collector current, a higher current gain of 246, and a lower base–emitter (B–E) turn-on voltage of 0.966 V at a current level of 1 μA, attributed to the increased charge storage of minority carriers in the InGaAs/GaAs superlattice-base region by tunneling behavior. The low turn-on voltage can reduce the operating voltage and collector–emitter offset voltage for low power consumption in circuit applications.

Keywords: InGaP/GaAs; Heterostructure emitter; Superlattice base; Turn-on voltage; Offset voltage

1. Introduction

GaAs-based heterojunction bipolar transistors (HBTs) have emerged to be one of the promising high-speed devices because of their expected potential based on a high current gain, a high current-handing capability, and an extremely high-frequency performance [1]. Typically, a relatively large base–emitter (B–E) turn-on voltage severely limits the minimum operated voltage and causes a large collector–emitter offset voltage (ΔV_{CE}), which increases the power consumption in circuit applications [2,3].

Over the past years, some approaches have been used to reduce the B–E turn-on voltage. One approach is to adopt a small energy-gap n-type emitter layer between confinement and base layers for eliminating the spike barrier blocking the electron injection from the emitter to the base [4–6]. Nevertheless, if the small energy-gap emitter layer is too thick, the transistor will perform with inferior confinement effect. Then, the charge storage in the neutral-emitter region enhances the base recombination current and increases the total base current [6]. On the other hand, if a thinner as well as small energy-gap emitter layer is employed, the device will serve as a conventional HBT and the turn-on is still considerably large. Another approach is to use a low energy-gap material as base layer [7–10]. Though InGaAs and GaAsSb ternary alloys have lower energy gap to control and improve the turn-on voltage, these introduce compressive strain and the layer thickness is critical due to a lattice mismatch with GaAs material. For the strain relation effects, the InGaAs quantum-well-based heterojunction as phototransistor has already been reported [11]. Furthermore, the use of the $In_xGa_{1-x}As_{1-y}N_y$ as base layer was well demonstrated to further reduce the energy gap in the base region and it effectively improved the problem associated with excess strain [9]. However, the blocking effect of collector current at the base–collector heterojunction could introduce a large knee voltage reducing the collector current.

In this article, a new InGaP/GaAs heterostructure-emitter bipolar transistor (HEBT) with InGaAs/GaAs superlattice-base structure is first reported and demonstrated. The addition of a thinner as well as small energy-gap emitter layer eliminates the potential spike at B–E

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junction, and the average energy gap in the base region is decreased by the use of the superlattice-base structure. As compared with the traditional HEBT, the minority charge storage in the superlattice-base region is enhanced and the collector current is substantially increased.

2. Device structures

The device structure of the superlattice-base device (labeled device A) includes a 0.5 μm $n^+ = 1\times10^{19}\,cm^{-3}$ GaAs subcollector layer, a 0.5 μm $n^- = 5\times10^{16}\,cm^{-3}$ GaAs collector layer, a $p^+ = 5\times10^{18}\,cm^{-3}$ InGaAs/GaAs superlattice base, a 300 Å $n = 5\times10^{17}\,cm^{-3}$ GaAs emitter layer, a 0.1 μm $n = 5\times10^{17}\,cm^{-3}$ $In_{0.49}Ga_{0.51}P$ confinement layer, and a 0.3 μm $n^+ = 1\times10^{19}\,cm^{-3}$ GaAs cap layer. The superlattice base consists of ten-period 50 Å $In_{0.2}Ga_{0.8}As$ layers and nine-period 50 Å GaAs layers. The conventional InGaP/GaAs HEBT (labeled device B) has a structure similar to device A, except that a 950 Å $p^+ = 5\times10^{18}\,cm^{-3}$ GaAs bulk base layer is employed to replace the superlattice base. A two-dimensional (2D) semiconductor simulation package SILVACO was used to analyze the energy band, distributions of electrons and holes, and dc performances of the two devices [12]. The 2D analysis takes into account the Poisson equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously. The emitter and collector areas are 50×50 and $100\times100\,\mu m^2$, respectively.

3. Results and discussion

The energy band diagrams near the B–E junction for devices A and B are illustrated in Figs. 1(a) and (b), respectively. Obviously, the potential spikes at the B–E junction of both devices are completely eliminated, even at $V_{EB} = 1.0$ V. The employment of a thin n-GaAs emitter layer between confinement and base layers enables the pn junction to act as a homojunction and helps to lower the energy band at the emitter side for eliminating the potential spike.

Fig. 2 shows the simulated common-emitter current–voltage (*I–V*) characteristics of the two devices at room temperature. Clearly, device A exhibits a higher collector current and a larger current gain than device B. An enlarged view near the origin of the *I–V* characteristics is depicted in Fig. 2(b). As seen in the figure, a relatively lower offset voltage of 16 mV at $I_B = 50\,\mu A$ is observed for device A, while device B shows a larger value of about 40 mV. Fig. 3 depicts the calculated Gummel plots of the two devices at $V_{BC} = 0$ V. The E–B turn-on voltage of device A is 0.966 V at the current level of 1 μA, which is 40 mV lower than the 1.006 V in the traditional HEBT. The low E–B turn-on voltage can reduce the operating voltage and collector–emitter offset voltage for substantially decreasing the power consumption in circuit applications. The current gains are 246 and 70 at $V_{BE} = 1.25$ V for devices A and B, respectively. In both devices, the ideality factor n_c for collector current is nearly equal to unity at low

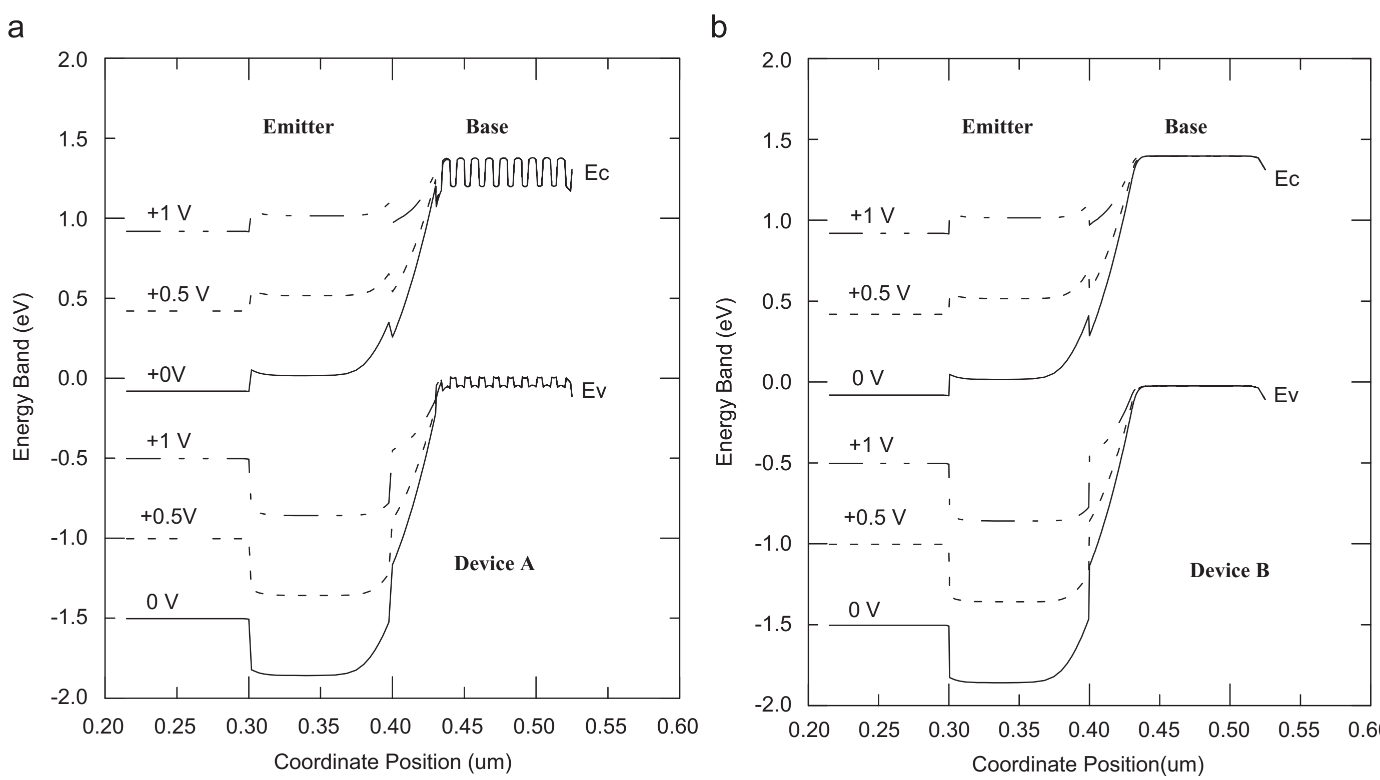

Fig. 1. Energy band diagrams near the base–emitter junction of (a) device A and (b) device B. Devices A and B represent the heterostructure-emitter bipolar transistors with and without the superlattice-base structures, respectively.