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Power dissipation sources and possible control techniques in ultra deep submicron CMOS technologies

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Abstract

As technology scales down into the ultra deep-submicron (UDSM) region, the static power dissipations grow exponentially and become an increasingly dominant component of the total power dissipation in CMOS circuits. With increase in gate leakage current resulting from thinner gate oxides in UDSM and the problems associated with short channel effects, leakage power dissipation is becoming a huge factor challenging a continuous success of CMOS technology in the semiconductor industry. With strict limitations of maximum allowable power (the power being limited more by system level cooling and test constraints than packaging) of 2.8 W (in 2005) to 3 W (in 2020) for battery (low cost/handheld) operated devices as projected by the *International Technology Roadmap for Semiconductors* (ITRS) 2005, innovations in leakage control and management are urgently needed. This paper presents an overview of the sources of the power dissipation mechanisms in the UDSM technologies, and the device and circuit techniques to control them.
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Keywords: Power dissipation; Control techniques; Submicron CMOS; Leakage current; Semiconductor roadmap

1. Introduction

The evolution of CMOS integrated circuit is a major milestone in the history of modern industry. It has driven a revolution in computing capability due to a long trend in increased performance, higher device density, and lower cost with scaling [1]. As the technology scales down to the ultra deep-submicron (UDSM), there are number of challenges to the continuing success of CMOS in the semiconductor industry. These challenges fall into the broad categories of reliability, variability, signal integrity, speed, and power problems [2]. Over the years, enhancing chip performance has come through increased circuit complexity and number of transistors. But despite down scaling of circuit propagation delay, supply and threshold voltages for every technology generation, the power dissipation in circuits has continued to increase. This increase is costly in terms of shorter battery life, complex cooling and packaging methods, and degradation of system performance.

Power dissipation in CMOS circuits involves both static and dynamic power dissipations [3]. In the submicron technologies, the static power dissipation, caused by leakage currents and subthreshold currents contribute a small percentage to the total power consumption, while the dynamic power dissipation, resulting from charging and discharging of parasitic capacitive loads of interconnects and devices dominates the overall power consumption. But as technologies scale down to the UDSM (see Fig. 1[4,5]), the static power dissipation becomes more dominant than the dynamic power consumption [1]. And despite the aggressive downscaling of device dimensions and reductions of supply voltages, which reduce the power consumption of the individual transistors, the exponential increase of operating frequencies results in a steady increase of the total power consumption. Eq. (1) gives the relationship between dynamic power consumption (P), capacitance (C), frequency (f), technology factor (k) and V_{dd} [1,5].

$$P = k.C.f.V_{dd}^2 \tag{1}$$

Based on data from the ITRS 2005 [6], this trend would continue as feature sizes of transistors continue to scale

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down. Consequently, if power dissipation, especially the static power dissipation, is not controlled and optimised carefully, it promises to become a major limiting factor for system integration and performance improvement [7–14].

Transistors consume static power when they are not switched ON having a small, so called leakage current flowing through them [8]. Over the years, this leakage current has continued to increase as technology scales down (Fig. 2) even though the OFF resistance of the devices decreases. Potential problems and challenges associated with leakage currents are many and vary with applications. Some of them are the requirements for sophisticated cooling methods, large battery sources and management of dynamic noise immunity. These factors adversely affect applications especially in portable and wireless electronic devices. Eq. (2) [1] gives the standby power of a CMOS chip due to source-to-drain subthreshold leakage.

$$P_{off} = W_{tot} V_{dd} I_{off} = W_{tot} V_{dd} I_O \exp\left(-\frac{qV_{th}}{mkT}\right), \quad (2)$$

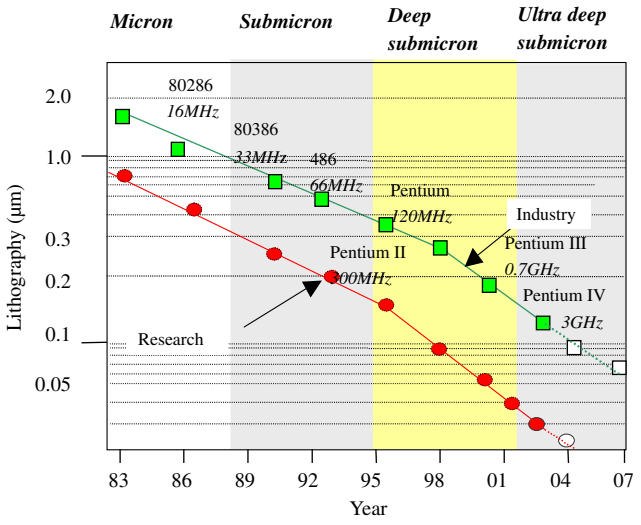

Fig. 1. Evolution of lithography [4,5].

where W_{tot} is the total turned-off device width with V_{dd} across the source and drain, I_{off} is the average off-current per device width, I_0 is the extrapolated current per width at threshold voltage, m is a dimensional factor, and V_{th} is the threshold voltage.

This paper is organized as follows: brief summary of 2005–2020 power supply and power dissipation roadmap is discussed in Section 2; Section 3 discusses the sources of leakage current in CMOS circuits. Section 4 discusses the leakage control techniques and Section 5 gives the final conclusions.

2. Brief Summary of 2005–2020 power supply and power dissipation roadmap

Table 1 shows the 2005–2020 Roadmap for power supply and power dissipation for CMOS circuits obtained from the ITRS 2005 [6]. As technology scales, strict limitation of the allowable maximum power for battery (low cost/handheld) operated systems is projected; from 2.8W in 2005 to only 3W in 2020. Within this period, the V_{dd} for high performance systems is expected to scale down by 36% while the allowable maximum power for high performance (with heatsink) devices will increase by only 19%. Short channel effects and gate leakage current would become very prominent in the UDSM due to shorter

Table 1
Roadmap trends 2005–2020 for power supply and power dissipation [6]

Chip characteristics/Production year	2005	2006	2008	2013	2016	2020
Power supply voltage (V)						
V_{dd} (high performance)	1.1	1.1	1.0	0.9	0.8	0.7
V_{dd} (low operating power, high vdd transistors)	0.9	0.9	0.8	0.6	0.5	0.5
Allowable maximum power (W)						
High performance with heatsink	167	180	198	198	198	198
Cost-performance	91	98	111	137	151	157
Battery—(low cost/handheld)	2.8	3.0	3.0	3.0	3.0	3.0

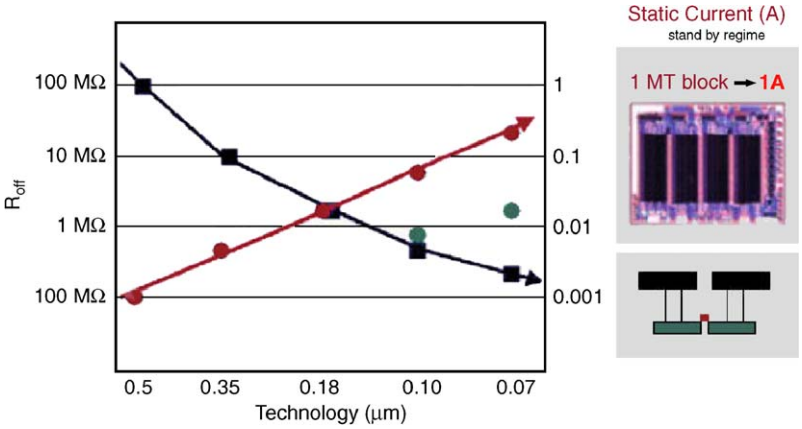

Fig. 2. Scaling of static current and OFF resistance of CMOS transistor [4].

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