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# High linearity CMOS mixer for domotic 5 GHz WLAN sliding-IF receivers

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**Abstract**

The present paper describes the design of a 1.1 GHz CMOS, fully differential, down conversion mixer to be used as a second down conversion mixer in an integrated transceiver for 5 GHz domotic WLAN. The circuit was implemented in a 0.35 μm SiGe BiCMOS technology and designed with the aim of getting high linearity without excessive reduction in the conversion gain. The obtained circuit exhibits a conversion gain of −1 dB and a third-order input intercept point of +10 dBm. Biased at 3 V, it dissipates 45 mW.


*Keywords:* CMOS; Mixer; Design; Characterization; Linearity

## 1. Introduction

A large interest is emerged during the last years in the design of RFIC's for IEEE 802.11a transceivers [1–7]. Thanks to its high data rate capability the IEEE 802.11a standard is well suited for high-quality audio and video transmission [8] with great potentialities in domotic scenarios [9]. For the implementation of these systems the availability of low-cost, small-size IEEE802.11a/HyperLAN2 integrated transceivers is of paramount importance.

The IEEE 802.11a standard requires ortogonal frequency division multiplexing (OFDM) modulation scheme, that exhibits high robustness against the multipath interference. Under the RFIC designer point of view, the OFDM modulation scheme complicates the transceiver design, specially when high-order QAM constellations are addressed as required for high rate transmissions, since it forces to get stringent performance on phase noise, I/Q matching, and dynamic range.

In particular, the receiver linearity becomes a critical issue, because of the high crest factor intrinsic in the OFDM modulation scheme. The mixers play a very important role in determining the linearity of the reception chain, because the in-band intereferers amplified by the LNA can produce high intermodulation products when processed by a not linear enough mixer.

The present work reports on the design of a 1.1 GHz CMOS mixer employed as the second down conversion mixer in a sliding-IF 5 GHz WLAN transceiver for domotic applications (see Fig. 1). It is here worth pointing out that even if the sliding-IF architecture has not been largely investigated in the literature [6,10], it does avoid the difficulties intrinsic in a direct conversion architecture (e.g. local oscillator emission and 1/f noise) offering, at the same time, the advantage of requiring one synthesizer only as pointed out in Fig. 1. In the present work, the second down conversion mixer was designed paying attention to get high linearity and keeping at the same time the conversion gain as high as possible. The passive mixers were therefore not considered as a possible solution in spite of their excellent linearity, because of their low conversion gains. A Gilbert cell was adopted, because a double balanced architecture generates low even-order harmonic distortion.

The paper is organized as follows: Section 2 describes the mixer design, Section 3 reports the experimental results, Section 4 compares the obtained performance with the literature, and, eventually, Section 5 draws the conclusions.

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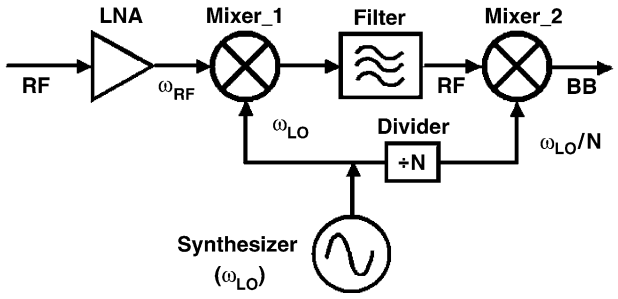


Fig. 1. Sliding-IF receiver architecture.

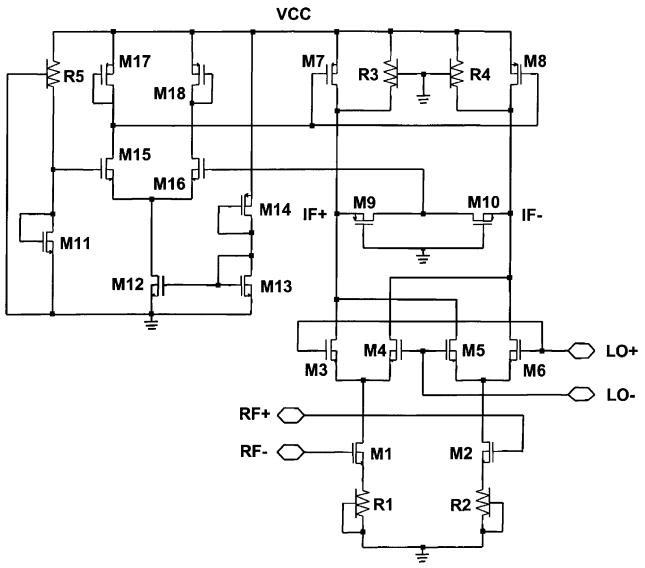


Fig. 2. Schematic of the designed mixer.

## 2. Design

The mixer, whose schematic is depicted in Fig. 2, was designed using a 0.35 μm SiGe BiCMOS technology so that it can be monolithically integrated on the same die with other building blocks, that can be usefully designed using high performance SiGe Heterojunction Bipolar Transistor available in this technology (e.g. the LNA in the receiver chain or the power amplifier pre-driver in the transmission chain).

All the MOSFET's are n-channel with exception of M7, M8, M17, and M18, which are PMOS. The common source M1 and M2 MOSFET's are the RF transconductor; they are resistive degenerated, to improve the linearity. No inductors were employed, in order to save space, even if their use allows better noise performance. It is worth pointing out that the noise figure is not a critical figure-of-merit, since the mixer is the last building block in the receiver chain (see Fig. 1).

The M3–M6 MOSFET's act as switches driven by the local oscillator (LO).

The load of a Gilbert cell can be made active [11–13, 15–17] or passive [14,15,18–21], differential [11–15,18,19] or single-ended [14,16,17,20,21]. As an alternative to the previous cited solutions, the present work adopted single-ended loads obtained using both active and passive components. On each branch of the Gilbert cell, the PMOS transistors (M7 and M8) were connected in parallel with resistors (R3 and R4). As in the case of the passive differential load, these resistors allow to improve the mixer linearity by reducing the mixer output impedance [12]. On the mixer branch where the switching transistors of the quad (M3, M4, M5, M6 in Fig. 2) are on, the transconductor transistors (M1 and M2 in Fig. 2) drive the active–passive loads (couples M7-R3 and M8-R4 in Fig. 2). Once the transistors in the quad are assimilated to ideal switches, the situation can be essentially captured by an inverter, as depicted in the inset of Fig. 3. The $V_{CMFB}$ voltage, controlling the mixer bias point, is generated by a common mode feedback bias (CMFB) constituted by a differential amplifier, whose core are the M15–M18 devices, that compares the reference voltage generated by M11 and R5 with the voltage sensed by the M9 and M10 transistors, that sense only the DC common mode without participating to the differential load. Transistors were used instead of resistors, in order to save silicon area.

The $Vx$ voltage corresponds to the voltage on the IF nodes of Fig. 2. Its swing is therefore the output voltage swing and it is strictly related to the mixer gain, as a consequence. On the gate of the NMOS transconductor the $V_{DC}+v_{RF}$ voltage is applied, where the $V_{DC}$ is the bias and the $v_{RF}$ is the incoming RF signal to be frequency converted. The transconductor provides at the output the $I_{DC}+i_{RF}$ current exciting the active–passive load.

In Fig. 3, the $I$–$V$ characteristics of a pure active load (open circles), of a pure passive load (open squares), and of the active–passive load used in the present work (open diamonds) are superposed on the NMOS output characteristics (black curves). By entering on the $y$-axis with the $I_{DC}+i_{RF}$ current the $V_X$ voltage swing, and therefore the gain, is determined by the $I$-$V$ load characteristic slope. In the case of a pure active load (open circles) a small RF current swing ($i_{RF}$) is enough to get a very large swing but

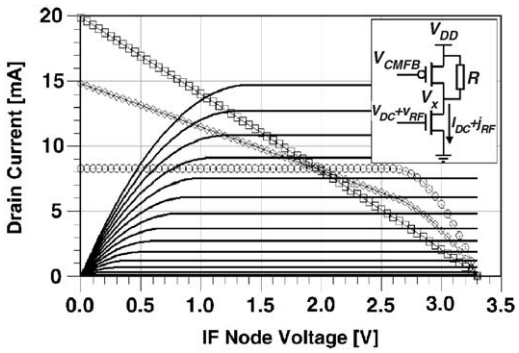


Fig. 3. Basic idea behind the adopted passive–active load solution. The black curves are the NMOS output characteristics; the open circles, squares, and diamonds are the characteristics of a pure active, pure passive, and active–passive load, respectively. In the circuit in the inset the degeneration resistors ($R_1$ and $R_2$ in Fig. 2) are not reported, because they are not essential to the idea description.