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Thermal management of electronic devices by composite materials integrated in silicon ☆

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ABSTRACT

As the power of electronic systems is increasing, thermal fluxes are getting higher, up to more than 100 W/cm^2 in the more critical cases. They result in hot spots with various consequences, especially performance reduction and reliability issues. Most of the prior research has been focused on active liquid cooling and on reducing hot spots by the implementation of thermal interface materials (TIMs) and spreading solutions.

The approach presented here is based on the implementation in silicon of nanocomposite structures including carbon nanotubes (CNTs) and phase change materials (PCMs). The simulation model presented here shows how the composite CNTs/PCM structure efficiently reduces the temperature excursion at the silicon surface compared to the implementation of PCM only or a thicker silicon. A fabrication process flow is presented with a special focus on the assembly of silicon top and bottom parts with CNTs. Process conditions are explored to insure mechanical adhesion and thermal contact quality. This thermal interposer concept provides a new solution for thermal management and reliability improvement of devices. It is of great interest for electronic and optical devices, MEMS and 3D integration.

1. Introduction

The increasing power of microelectronic devices following Moore's law raises heat dissipation challenges. Added to that, 3D heterogeneous integration is developed to extent module complexity and address heterogeneous integration of new components. This "More than Moore" approach drastically increases the thermal challenges, especially when dies are implemented in portable devices. In confined environments, transient thermal fluxes can generate severe hot spots which can impact device reliability or performances.

Previous research on thermal management has been focused so far on thermal spreaders or TIMs [1] which are both passive solutions with some limitations. Active solutions like fluid circulation in microchannels have been developed successfully [2] in terms of performance, but their complexity has limited their deployment for portable devices. Little work has been done on solid/liquid phase change materials (PCMs) which are able to absorb the latent thermal energy corresponding to their phase change enthalpy [3]. PCMs have faced implementation problems in practical applications because most of them have a low thermal conductivity which creates high thermal resistance paths.

The solution presented in this paper is based on an innovative architecture of a silicon interposer in which a nanocomposite structure is imbedded. This material is based on CNT cells filled with a phase change material. A quite large amount of thermal energy can be stored in the phase change enthalpy of the PCM while the CNT structure provides a high thermal conductivity of the composite material. This paper presents both a simulation model of the composite thermal interposer and a focus on critical process steps needed to build the interposer.

2. Concept and model

The proposed thermal interposer concept is presented in Fig. 1. A cavity is etched in silicon and a composite structure made of CNT

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cells and PCM is embedded into the cavity which is closed by a second silicon part. When a heat spike occurs at the top surface, the heat is transmitted into the composite structure and one part of it is absorbed into the phase change enthalpy at the phase change temperature. The temperature increase is consequently limited. The CNT structure drives the thermal flux into the PCM and also reduces the thermal resistance of the whole composite structure. As a consequence, the whole structure keeps the ability to transmit the nominal heat flux when the environment operates below the phase change temperature.

The following sections present the structure used for the 2D time dependent simulation and then the results in the case of a high thermal transient flux applied on one side of the structure.

2.1. Geometry and model

The structure used for the simulation is presented in Fig. 2. It includes a 2.5 μm thick wall made of dense CNTs surrounded by a 100 μm large PCM cell. The height of the composite PCM/CNTs structure is 100 μm. The silicon base and cover parts are 100 μm thick. A symmetry condition has been applied to the left and right sides of the structure.

Multiphysic simulation (Comsol software) has been conducted to estimate the efficiency of the concept in terms of thermal management, especially compared to alternative potential solutions: increase silicon thickness or introduce only PCM in silicon. The thermophysical properties of the materials used are summarized in Table 1.

The enthalpy of the phase change is supposed to be $\Delta H = 250\ \mathrm{kJ\cdot kg^{-1}}$. The PCM properties are representative of an alkane paraffin [4]. The phase change is supposed to occur between $T_1 = 80\ ^\circ\mathrm{C}$ and $T_2 = 82\ ^\circ\mathrm{C}$. The phase change is modeled by the following function of the specific heat Cp:

$Cp_s = 2100\ \mathrm{J\cdot kg^{-1}\cdot K^{-1}}$ if $T < 80\ ^\circ\mathrm{C}$ (solid).
$Cp_l = 2300\ \mathrm{J\cdot kg^{-1}\cdot K^{-1}}$ if $T > 82\ ^\circ\mathrm{C}$ (liquid status).
$Cp_t = \Delta H/(T_2 - T_1) + (Cp_s + Cp_l)/2$ if $80\ ^\circ\mathrm{C} < T < 82\ ^\circ\mathrm{C}$ (phase transition).

The model is based on conductive heat transfer inside the structure. Convective heat transfer and surface to ambient radiation conditions are applied at the top surface. The transfer coefficient h is supposed to be $10\ \mathrm{W\cdot m^{-2}\cdot K^{-1}}$ and the emissivity 0.9. The heat transfer coefficient of the bottom surface is supposed to be $2000\ \mathrm{W\cdot m^{-2}\cdot K^{-1}}$ representing an efficient thermal extraction path to the ambient. Thermal contact resistances between silicon and CNTs are neglected in this simulation. The heat generation at the top surface is modeled by a heat source of $1e6\ \mathrm{W\cdot m^{-2}}$ ($100\ \mathrm{W\cdot cm^{-2}}$) during 20 ms. These values are typical of severe hot spots in electronic circuits. Their thermal fluxes or durations can vary depending on devices or use cases. The initial temperature is set at 75 °C.

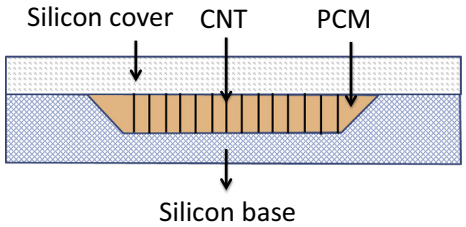

Fig. 1. Principle of the thermal interposer.

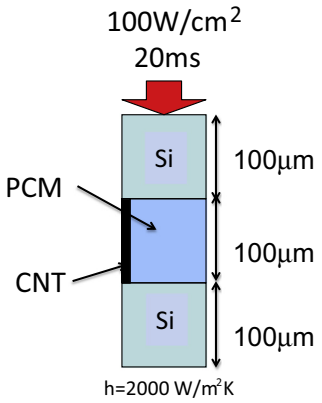

Fig. 2. Simulated composite structure.

2.2. Simulation results

The evolution of the top surface average temperature as a function of time after a 20 ms heat pulse is shown in Fig. 3. This top silicon surface is representative of an active device generating heat. Three cases are presented with the following hypotheses regarding the material of the cavity: all silicon, PCM only, composite PCM/CNTs structure.

The case of Si only represents a potential possible solution of thermal management by increasing the silicon die thickness to spread the heat in a larger volume. In this case, the surface temperature increases very fast up to 110 °C which is very close to the limit admitted for logic junctions (~125 °C) and far upper than the one admitted for memory devices (~85 °C). The introduction of only PCM in the cavity results in a worse solution even if some energy is transferred in the phase change. The reason is linked to the low thermal conductivity of most PCMs having a high phase change enthalpy. The PCM results in a high thermal resistance path and the temperature increases up to 135 °C. The solution of the composite PCM/CNTs structure is the most efficient one. The temperature of the surface only reaches 96 °C, and decreases very fast after the spike thanks to the heat absorption in the PCM. The thermal conduction between upper and lower silicon surfaces thanks to the CNTs structure also allows a faster extraction of the heat from the PCM. Consequently, the hybrid structure allows a fast PCM recovery before the next thermal pulse. Fig. 4 shows the temperature mapping across the interposer after 20 ms, corresponding to the end of the heat pulse.

In the case of Si, the temperature increase is limited by the spreading in the silicon volume (sensible heat). When the cavity is only filled with PCM, the temperature increases very fast because of the low thermal conductivity of the PCM layer. Even if some heat is absorbed in the transition, this is only limited to the upper surface and heat cannot flow downward in silicon. When PCM/CNTs are implemented, the heat can flow across the structure. A higher contact surface with the PCM allows a higher volume to be melted as well as some spreading towards the base silicon. This results in a high performance thermal management.

3. Interposer building blocks

This section first describes the process flow developed to build the thermal interposer. Critical steps like CNTs growth in cavities and PCM choice are highlighted. Then, the assembly of silicon base/CNTs/silicon cover is detailed as it is very critical to insure mechanical integrity as well as low thermal resistance of the interposer.