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Fabrication of double recess structure by single lithography step using silicon-nitride-assisted process in pseudomorphic HEMTs

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ABSTRACT

Monolithic microwave integrated circuits (MMICs) play an important part in today's wireless communication electronics. GaAs-based pseudomorphic High Electron Mobility Transistor (pHEMT) is used in MMIC-based low noise amplifier (LNA) and power amplifier (PA) stages. The latter requires high device current (I_{ds}) and high reverse breakdown voltage (BV_{gd}). In addition, the ON-state breakdown voltage should be high enough to operate the device at higher source–drain voltage (V_{ds}). Double gate recessing is a well-established technique used to increase the ON and OFF-state breakdown voltages of a pHEMT device for power applications, which requires two levels of masking and recessing. In this paper, we present a single mask processing technique for realizing double recess structure with the help of silicon nitride layer. The new process involves deposition of silicon nitride after mesa isolation step of device fabrication. After gate lithography, two etching steps of silicon nitride and GaAs, followed one after the other, generates the double recess structure, wherein the various etch times decide the width and shape of double recess structure. The electric field distribution at the Schottky interface as well as along the channel has been simulated using ATLAS for the double recess structure used in this work. The fabricated recess structure showed improvement in breakdown voltage of the device which has been correlated to the effective redistribution of electric field in the device, as shown by simulation.

1. Introduction

PHEMT-based power amplifiers are used in RADAR and microwave communication systems [1–5]. The maximum drain current (I_{dmax}) decides the maximum output power from the device, and reverse bias breakdown voltage (BV_{gd}) provides the operational safety limits of the device. In addition, the ON-state breakdown voltage (BV_{on}) should be as high as possible in power pHEMTs in order to operate the device at higher voltages between source and drain (V_{ds}) [6]. The BV_{gd} is also important for pHEMTs used for switching application [7].

The reverse breakdown phenomenon of HEMT is essentially involving the leakage current across the Schottky gate barrier. Hence, the different mechanisms proposed to explain this phenomenon include thermionic field emission [8,9], tunneling [8,10–13] and impact ionization [13–15] across the depletion layer below gate electrode. These mechanisms are dependent on electric field at gate metal–AlGaAs interface, at gate edge towards drain, and can simultaneously occur under different operational conditions of the device. The ON-state breakdown in pHEMTs, on the other hand, is caused by impact ionization in the channel under high voltage bias condition across source and drain [13]. The ON-state breakdown voltage is dependent on the electric field distribution along the channel, especially between gate and drain which can be engineered by various methods like double recessing, introduction of field plate etc. [16]. Both BV_{gd} and BV_{on} can be controlled by tailoring the electric field profile at the Schottky gate and in the device channel respectively [17–20]. It has been experimentally reported that the widening of single recess structure leads to increase in BV_{gd} but does not increase the BV_{on} which points out that the mechanisms for both are different from each other [21].

Double recess structures, reported in literature, are generally fabricated by a two-mask process [22]. In the first mask, the wider gate opening is realized followed by a partial recess etch. In the second mask, the narrower gate lithography is done and recessing is performed for a shorter time. This approach requires two steps of

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lithography and recessing. Double recess structures have also been attempted in a single masking step by the following various methods: one method involves bi-layer lithography technique combined with reactive ion etching using two layers of resist and an additional layer of germanium [23]. Another method involving tri-layer e-beam lithography process using PMMA and P(MMA-MAA) resists has been successfully used to generate asymmetric double recess structure in pHEMTs [24]. A method comprising e-beam lithography using PMMA and P(MMA-MAA) along with PMGI resists and SiO_2 have also been used in the fabrication of asymmetric recess and T gate [25]. Similar work has also been reported in Metamorphic HEMT by using combination of PMMA and P(MMA/MAA) and PMGI resists [26]. The last three methods use multiple steps of e-beam exposures and developing to realize the necessary gate recess structure. A different technique for generating asymmetric gate recess grooves in InAlAs/InGaAs MODFETs using single masking process uses an electrochemical fabrication approach [27].

In contrast to the above methods, in this paper we propose a new method of double recess by a single layer of resist and single masking or lithography step. An additional silicon nitride layer has been used to generate the double recess structure by multiple etching sequences of silicon nitride and GaAs.

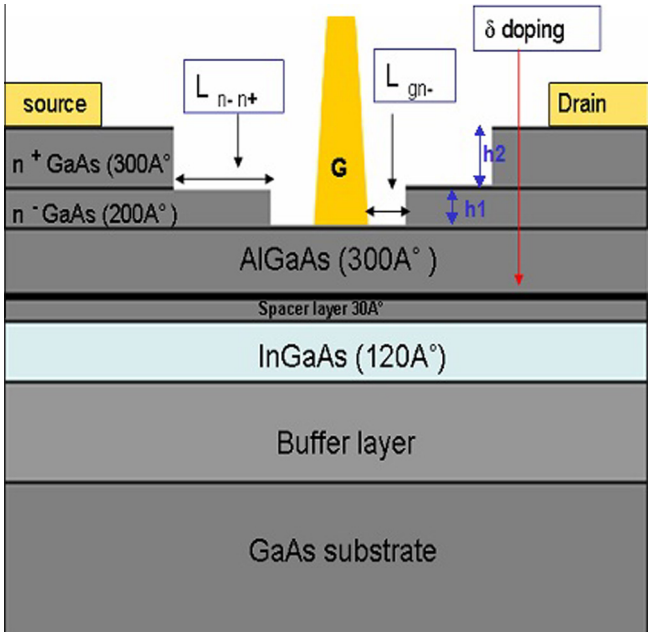

Fig. 1. Double recess HEMT structure.

2. Experimental

The pHEMT double recess structure used for study during this work is shown in Fig. 1. To facilitate the formation of double recess structure, the contact epilayers are grown with an n^+-GaAs layer with a carrier concentration of 5×10^{18} cm^{-3} and n^--GaAs layer with 1×10^{17} cm^{-3}.

In our experiments, a silicon nitride film covers the area between source and drain, followed by gate lithography as shown in Fig. 2(a). The silicon nitride in the gate opening portion is etched in buffered hydrofluoric acid (BHF) for time t_1 which generates some amount of lateral or sidewise etching, which is a function of time t_1 (Fig. 2(b)). The GaAs is etched using citric acid/H_2O_2-based etchant for time T_1 which generates a step height of h_1, as shown in Fig. 2(c). Next, silicon nitride is etched again for time t_2 to generate another level of lateral etch length in silicon nitride, as shown in Fig. 2(d). Then the second GaAs etching is performed for time T_2 to generate a step height of h_2, as shown in Fig. 2(e). Gate deposition and lift-off, as shown in Fig. 2(f), are carried out after these etching steps. In this approach, the gate length is decided by the photoresist opening on the top, and the double recess structure on either side of the gate is decided by the nitride etch. The nitride etch time t_1 decides the first recess width and the time t_2 decides the second recess width. Depending upon the thickness of n^+ and n^- layers, the times T_1 and T_2 are adjusted in such a way that height h_1 is the thickness of n^--GaAs and height and h_2 is the thickness of n^+-GaAs.

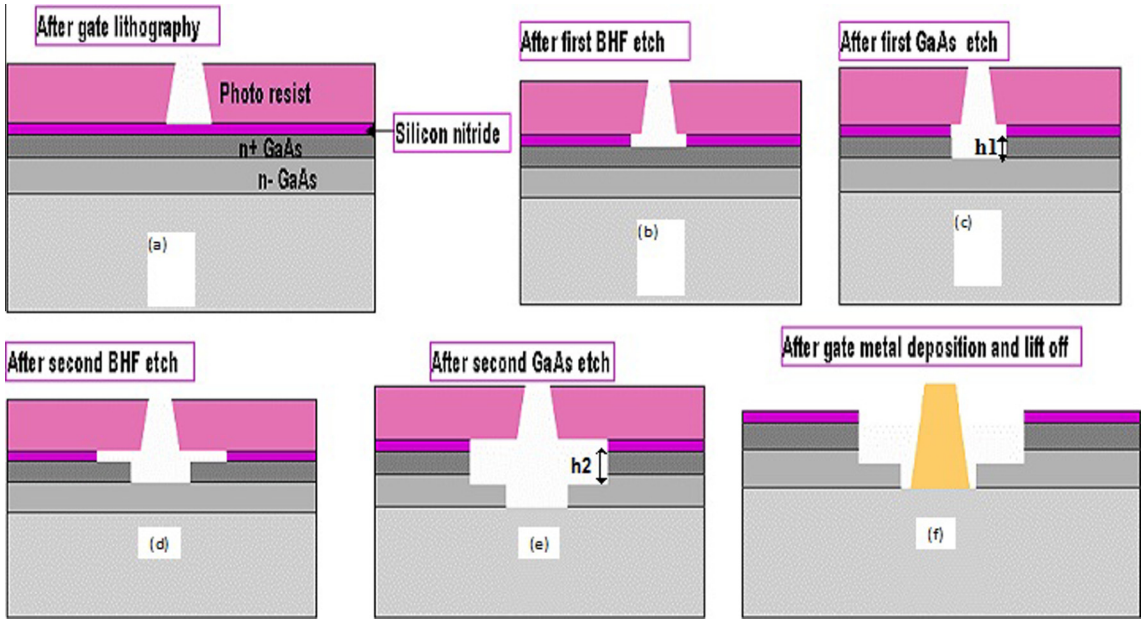

Fig. 2. Gate opening cross section (a) after gate lithography, (b) after first BHF etch for time t_1, (c) after GaAs etch for time T_1, (d) after second BHF etch for time t_2, (e) after second GaAs etch for time T_2 and (f) after gate metal deposition and lift-off.